

Low Power Architecture and FPGA Design for Effective Detection of Recycled IC

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Abstract

Owing to the socialization of the semiconductor design and fabrication process, integrated circuits (ICs) are becoming more susceptible to malicious activities. The unauthentic and reusing of integrated circuits have become foremost issues in upcoming years. The two types of on-chip lightweight sensors are proposed to recognize recycled ICs by measuring circuit usage time when used in the field. Recycled ICs detection based on aging in RO (ring oscillator) based sensor is used to analyze the aging effect and in AF(anti fuse) based sensor counts the cycle of system clock or switching activities of nets. The Sequential Optimization Algorithm is proposed to efficiently distinguish the forged and recycled ICs and ingests less power compared to the conventional method. The proposed method is designed using Verilog HDL, simulated using Modelsim and synthesized using Xilinx Software.

1. Introduction

An Integrated circuit is an electronic circuit on one small chip of semiconductor material. The recycled ICs are the main issues related to the protection of ICs for many years. The forging of ICS is the important problem that affects the reliability of electronic systems. A forged component is an electronic part that is simply fake because it: (i) is an uncertified copy; (ii) is not manufactured by the original component designer; (iii) has wrong documentation. It is shown in [1] that recycled products account for 80 to 90% of all forges being sold worldwide. Hence, it is necessary to prevent recycled ICs from involving in crucial infrastructure as they fail earlier than new chips.

The improvement of techniques for recycled ICs detection is the major considerations. Since it is used prior in the market, the performance of the ICs must have been affected. This performance degradation is used to identify recycled ICs. The recycled ICs issue and detection can be handled using light weight on chip sensors. These sensors are the primary attempt to solve recycled ICs issue. The components in the sensor which are placed next to each other is the key to identify the impact of aging effects that are formed by the process variations. With less area coverage, these sensors are identified to be very effective. The on chip light weight sensors basically used are Ring oscillator sensor and antifuse sensor. The ring oscillator sensor detects the recycled IC by analysing the aging effects. The Antifuse sensor is generally two types. They are Clock based antifuse sensor and Signal antifuse based sensor. These sensor identifies the recycled IC by counting the clock and from switching activities of the nets.

2. Literature Survey

Baumgarten A, Tyagi A, and Zambreno J (2010) proposed "Preventing IC piracy using reconfigurable logic barriers". It uses Hardware metering technique. The hardware metering can be passive or active. The Passive

approach identifies each IC and then suspected ICs are checked. A combinational-locking scheme is integrated into a standard CAD tool flow to prevent IC piracy. The Active approach locks each IC until it is unlocked by the IP holder. Here, the logic barriers separate the inputs from the outputs and each path goes through the barrier. The combinational locking scheme is used to guide logic barriers, so that logic barriers block the information for incorrect key. The overproduction of ICs will be prohibited and authenticates the ICs effectively. But it does not detect the recycled ICs if they have same IDs as unused ICs. Daasch W R, Lofstrom K, and Taylor D (2000) proposed "IC identification circuit using device mismatch". It uses the array of addressable MOSFETs and auto zeroing comparator. Due to device mismatch, the drain currents will be randomly different, producing a sequence of random voltages. The auto zeroing comparator converts the random voltage sequence in to a binary identification sequence. The Hamming distance between two ID bit sequence is calculated. The IDs are stored in the database and single ID is compared with original ID whose distance should be small. It does not require a special processing or after-fabrication programming. But there is a lack of IC identification when there is a change in the identification bits. Karraker D and Stradley J (2006) proposed "The electronic part supply chain and risks of counterfeit parts in defense applications". It presents the percentage of used ICs and the numbers relating to semiconductor sales and counterfeiting parts. The criteria for evaluation of electronic parts distributors such as handling, storage, corrective actions of counterfeit parts are discussed. The recommendations to be followed to ensure that trusted supply chains are available for policy decisions of the DOD are presented that helps in mitigating the risk on inclusion of counterfeit and other sub standard parts in the national security systems at the system integrator level. But it does not explain about the methods to detect counterfeit ICs. Keane J, Wang X, Persaud D, and Kim C H (2010) proposed "An all-in-one silicon odometer for separately monitoring HCI, BTI, and TDDB". It uses improved silicon odometer beat frequency measurement. This circuit contains four ROs in total two stressed, and two unstressed to

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maintain fresh reference points. It uses a “back drive” concept, in which one ROsc drives the voltage transitions in both structures during stress, such that the driving oscillator ages due to both BTI and HCI, while the other suffers from only BTI. The operation is similar to silicon odometers that consist of ring oscillator but the circuit is stressed after recording of about 3 results. This was done to monitor the stress conditions separately and fast frequency degradation measurement was achieved. But the design is more complicated. Kim T, Persaud R, and Kim C H (2008) proposed “Silicon odometer: An on chip reliability monitor for measuring frequency degradation of digital circuits”. It uses silicon odometers which consist of pair of ROs, phase comparator and counter. The one ring oscillator is stressed and the other operates in normal condition. The phase comparator uses the one of the RO clock as the input clock and operates in precharge or evaluation mode. The output of this phase comparator exhibits the beat frequency. To avoid mismatch, majority voting circuit is used. The counter calculates the percentage of the frequency degradation based on the beat frequency obtained from ring oscillators. Mahapatra S, Saha D, Varghese D, and Kumar P B (2006) proposed “On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress”. It uses the interface trap generation. It involves in breaking of Si-H bond and Si-O bond that is developed for NBTI, FN and HCI stress. The time evolution is governed by either one-dimensional or two-dimensional reaction-diffusion models. Hot holes break $\equiv\text{Si}-\text{O}$ bonds during both FN and HCI stress. This contribution is explored by HH and HE energies. The trap generation cannot be recovered during the breaking of Si-O bond under room temperature. Then the lifetime prediction of the device is done under stress condition. But it has high delay as it takes some time to recover from the stress. it does not measure the degradation in integrated circuits. Tehranipoor M and Zhang X (2012) proposed “Identification of recovered ICs using fingerprints from a light-weight on-chip sensor”. It uses ring oscillators for effectively detecting the recycled ICs. The Combating die recovery (CDR) sensor consists of stressed RO and reference RO and the frequency difference between them is calculated. Using statistical data analysis, process and temperature variations effects on the sensors can be separated from aging experienced by the sensors in the ICs when used in the field. The frequency difference should be small for good ICs. The aging analysis, process variation analysis is experimented and the measurement flow using CDR sensor is explained for identifying recovered ICs. But the analysis of usage time of IC is not accurate.

3. On Chip Light Weight Sensors

The two techniques using light weight sensors (RO-based and AF-based) detects the recycled ICs. The RO-based sensor consist of a reference RO and a stressed RO. The stressed RO has high aging rate where as the reference RO experiences less stress. The frequency difference between the two ROs used to obtain the usage time of the chip under test. If the difference is large, the CUT is found to be used one; else it is a new one. The AF (Antifuse) based sensor consists of counters and an embedded antifuse (AF) memory block. The counter records the usage time of

ICs and the address is stored in the AF memory block. The recyclers cannot track the content in AF memory.

3.1 Structure of Ro Based Sensor

This sensor detects the recycled ICs based on aging difference between stressed RO and Reference RO. It does not require additional memory element. The structure of RO based sensor, which is shown in fig.3.1, consist of control module, a reference RO, a stressed RO, a MUX, a timer and a counter. The cycle count of the ROs is measured by counter. The timer controls multiplexer. The timer uses the system clock and it is controlled by ROSEL signal. These ROs consist of chain of inverters and it can also be replaced by any other type of gates.

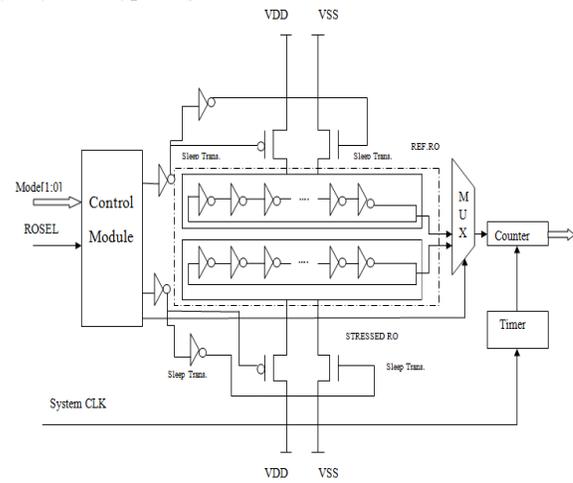


Fig. 1. Structure of the RO-based sensor

There are three modes of operation in this sensor. During manufacturing mode, both ROs will be disconnected from the power supply and they will not experience aging. During the normal functional mode, the stressed RO alone will be gated on and reference RO will be disconnected. During the authentication mode, both ROs will be gated on. When comparing to many number of gates, the area coverage of RO based sensor is negligible.

3.2 Structure of AF Based Sensor

The RO based sensor provides only approximate value of the usage time. This problem is overcome by using AF based sensor that provides accurate usage time and identifies recycled ICs though it is used for short period. The two AF based sensor are CAF based sensor and SAF based sensor.

3.2.1 Structure of CAF and SAF Based Sensor

The CAF based sensor consists of two counters, a dataread module, an adder and an AF OTP memory block. The counter1 divides the high frequency system clock to low frequency signal. The counter2 measures the cycle count of the low frequency signal. A AF memory block is a field programmable ROM that stores the usage time information. The dataread module controls MUX1. The Reg1 samples the data in the adder and Reg2 delays the data stored in the Reg1. The values in the register are compared and if they are different, the AF block will be in program mode. This structure is shown in fig 3.2. The area overhead in CAF based sensor is large and to overcome this problem

SAF based sensor can be used. This structure is shown in fig. 3.3. The structure of SAF based sensor is similar to the CAF based sensor but only the difference is one counter is replaced by AND gate. The input to the AND gate are certain number of nets. This nets are selected based on the rule that the switching activity of the AND gate output must meet measurement scale requirement.

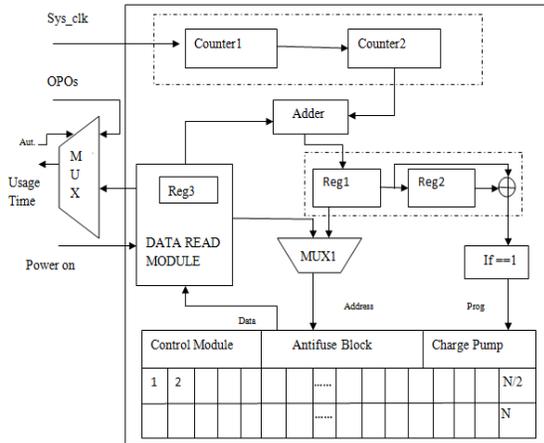


Fig. 2. Structure of CAF Based Sensor

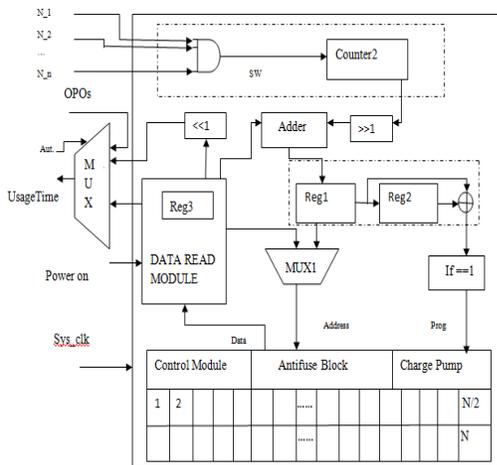


Fig. 3. Structure of SAF Based Sensor

4. Simulation and Synthesis Result

The simulation for Ring Oscillator (RO) and Antifuse(AF) sensor is done using Modelsim simulator. The simulation for ring oscillator sensor is shown in fig.4. The simulation for CAF based sensor is shown in fig. 5. The simulation for SAF based sensor is shown in fig. 6. The IC view, schematic view and power analysis can be obtained by synthesizing in Xilinx software. The IC view is shown in fig. 7. Synthesis report gives the efficient usage of number of flip-flops used and bonded IOBs, number of slices and register used. After performing the synthesize process, the RTL (Register Transfer Logic) Schematic has been created automatically based on the functionality. RTL schematic window is cross sectional of top view of IC. The routing between the different cells can be viewed clearly by this schematic. The technology window is front view of IC.

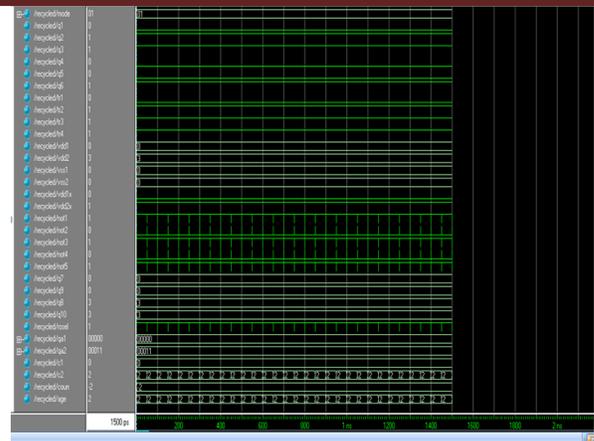


Fig. 4. Simulation of RO based sensor

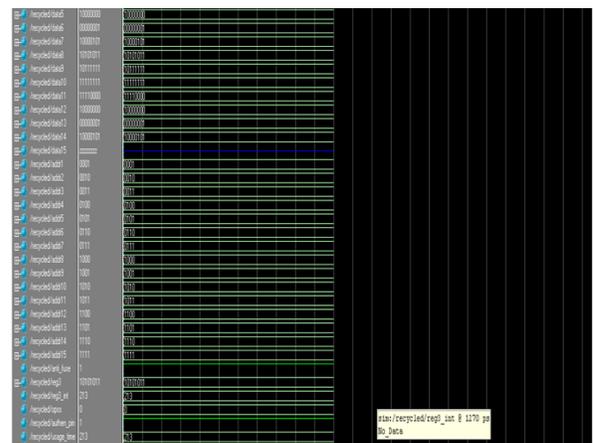


Fig. 5. Simulation result for CAF based sensor

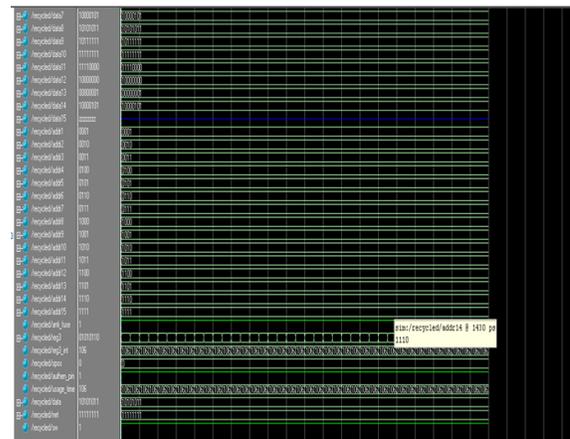


Fig. 6: Simulation result for SAF based sensor

RTL View is a Register Transfer Level graphical representation of our design. The goal of this view is to be as close as possible to the original HDL code. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design. In the RTL view, the design is represented in terms of macro blocks, such as adders, multipliers, and registers. Standard combinatorial logic is mapped onto logic gates, such as AND, NAND, and OR. This is shown in fig. 8.

The technology schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of LUTs, carry logic, I/O buffers, and other technology-specific components. Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture, which might help you discover design issues early in the design process. This is shown in fig. 9.

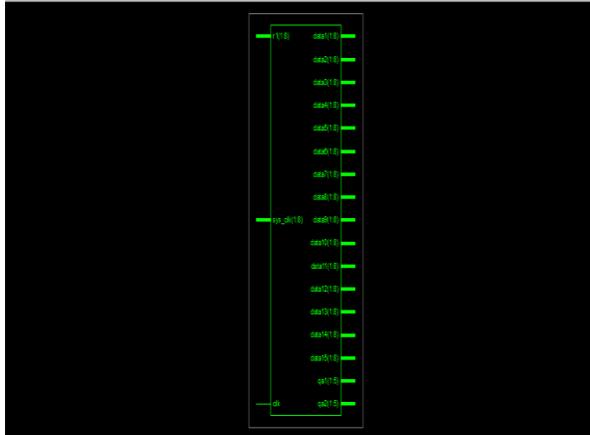


Fig. 7. IC View

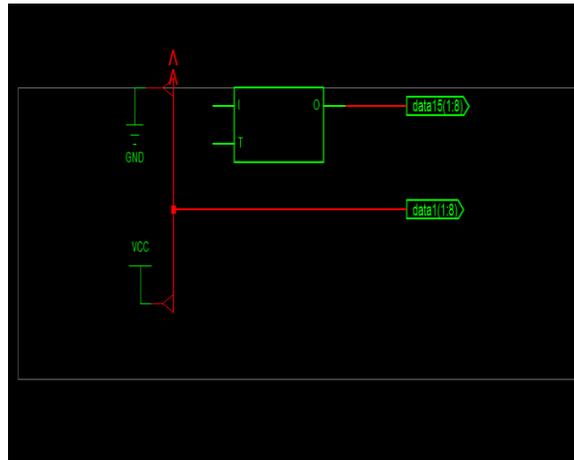


Fig. 8. RTL Schematic



Fig. 9. Technology Schematic

The power analysis is shown in Fig. 10. The total estimated power is 253 mW.

Mode	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2	0.00	0.00
Dynamic		0.00	0.00
Quiescent		45.85	55.81
Vccaux	2.5	0.00	0.00
Dynamic		0.00	0.00
Quiescent		77.25	193.13
Vcc025	2.5	0.00	0.00
Dynamic		0.00	0.00
Quiescent		0.00	0.00
Total Power			252.94
Startup Current		0.00	
Battery Capacity (mAh-Hour)		0.00	
Battery Life (Hours)		0.00	

Power summary:			
	I (mA)	P (mW)	
Total estimated power consumption: 253			

Vccint 1.20V:	50	60	
Vccaux 2.50V:	77	193	
Vcc025 2.50V:	0	0	

Logic:	0	0	
Outputs:			
Vcc025	0	0	
Signal:	0	0	

Quiescent Vccint 1.20V:	50	60	
Quiescent Vccaux 2.50V:	77	193	

Thermal summary:	
Estimated junction temperature:	30C
Ambient temp:	25C
Case temp:	30C
Theta J-A range:	21 - 18C/W

Analysis completed: Sun Nov 23 19:00:39 2014

Fig. 10. Power Analysis

5. Conclusion

There are two techniques that uses lightweight on-chip sensors to detect recycled ICs. The frequency difference between the reference and the stressed ROs in the RO-based sensor made the easy identification of recycled ICs possible. The usage time stored in the AF memory using AF based sensors could show how long an IC had been used and then identify a recycled IC. Experimental results and analysis demonstrated the effectiveness of these sensors. The Sequential Optimization Algorithm can be proposed that efficiently detects the recycled ICs which can be used in low power applications. The RO and AF sensors can be merged in to simplified architecture using this algorithm and the performance is analysed using Xilinx software and designed in FPGA and simulated in Modelsim software.

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