Low Power Efficient D-Latch Based Carry-Select Adder

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Abstract
The logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to study the data dependence and to identify redundant logic operations. The carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to cin = 0 and 1) and fixed cin bits are used for logic optimization of CS and generation units. The proposed CSLA design involves significantly less area and delay than the SQRT-based CSLA. The design of an efficient carry select adder using the single Ripple carry adder and D-latch is presented.

1. Introduction

Very large scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI is mainly applied for miniaturization of complex circuits so as to achieve better speed, reduce chip size, minimum power consumption and enhance better performance. This technology replaces older electronic components such as vacuum tubes, valves and resolves pitfalls exits in are, speed and power constraint.

2. Existing System

A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sum words and output carry bits corresponding the anticipated input-carry (cin =0 and 1) and selects one out of each pair for final-sum and final-output-carry. A square-root (SQRT)-CSLA to implement large bit-width adders with high delay

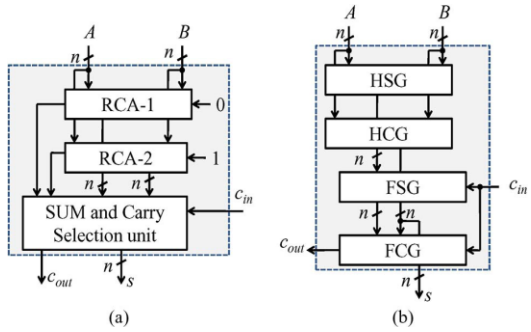

Fig: 1. Conventional CSLA; n is the Input Operand bit-Width

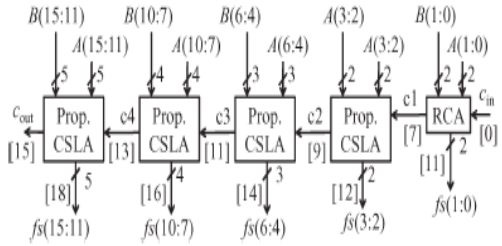

Fig: 2. SQRT-CSLA for n = 16

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3. Limitations

A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure

4. Proposed System

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power.

The design of an efficient carry select adder using the single Ripple carry adder and D-latch is presented.

Advantage

The proposed architecture, lends itself to aggressive voltage scaling for low-power dissipation. By the proposed using D-latch architecture, hardware complexity is reduced successfully and can gain the advantage in terms of area, power consumption and delay.

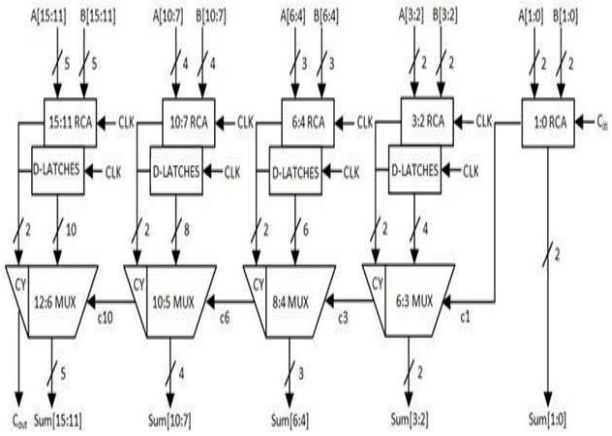

Fig: 3. Efficient Carry Select Adder using the Single Ripple Carry adder and D-latch

5. Software/Hardware Implmentation

Simulation Tool : Model Sim –Altera 6.4a.
Synthesis Tool : ALTERA – Quartus II
HDL : Verilog HDL

Application

LOW-POWER, area-efficient, and high-performance VLSIsystems are increasingly used in portable and mobiledevices, multistandard wireless receivers, and biomedical instrumentation. An adder is the main component of anarithmetic unit. A complex digital signal processing (DSP) system involves several adders.

6. Conclusion

A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. The proposed scheme reduces the delay, area and power compared to the regular and modified CSLA by the use of D-latches.

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