Integration of NOC Architecture with Classical Bus Based System

Manikandan. M, Ramya. R
Department of Electronics and Communication Engineering, Gnanamani College of Technology, Namakkal, Tamil Nadu, India

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Abstract
The increasing complexity of modern digital devices demands for ever increasing communication requirements, and for an ever increasing heterogeneity of the target applications. Specifically different communication domains may be implemented using the same chip area, for instance to allow multiple parallel applications to be loaded onto the device. Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in heterogeneous digital systems. Classical design approaches, such as bus-based systems or point-to-point connections, are no longer suitable for highly integrated systems since they lack of flexibility and scalability with the increasing number of modules attached to the system.. Such an issue can be solved by directly optimizing over the different design factors. What should be achieved is low-resource usage communication architecture, meanwhile maintaining the desired performances. In the proposed methodology Integration of NoC (Network on Chip) architecture with Classical Bus based systems to overcome the disadvantages of both Classical and Network based methodologies. The efficiency of the proposed methodology is shown by comparing with existing methodology, taking directly into consideration the resource requirements of the target FPGA device.

1. Introduction

Historically, computation has been expensive and communication cheap. With scaling microchip technologies, this changed. Computation is becoming ever cheaper, while communication encounters fundamental physical limitations such as time-of-flight of electrical signals, power use in driving long wires/cables, etc. In comparison with off-chip, on-chip communication is significantly cheaper. There is room for lots of wires on a chip. Thus the shift to single-chip systems has relaxed system communication problems. However on-chip wires do not scale in the same manner as transistors do and as we shall see in the following, the cost gap between computation and communication is widening. Meanwhile the differences between on- and off-chip wires make the direct scaling down of traditional multicomputer networks suboptimal for on-chip use.

1.1 On-Chipcommunication Architectures

This chapter gives the brief explanation about the various existing On-chip Communication architectures and finally the comparison between different On-chip communication architecture. On-chip communication infrastructure design paradigms can be easily classified into two main classes: bus-based and network-based. The first group employs a shared resource providing a centralized and controlled view of the physical channel, while network-based communication employs a set of distributed communication resources. Purpose of this section is to highlight the advantages and drawbacks of the two paradigms.

1.2 Classical Design Approaches

Classical design approaches are point-to-pinot and bus based architectures. This group employs a shared resource providing a centralised and controlled view of the physical channel.

Corresponding Author,
E-mail address: manikandanrasi@gmail.com

1.3 Bus Based Architectures

The most relevant efforts to realize bus-based systems for reconfigurable architectures are BUS-COM and *Reconfigurable Multiple Bus-on-Chip* (RMBoC). BUS-COM is divided into parallel channels as shown in Fig. Access to the shared medium is given by an arbiter, according to a static or dynamic slot assignment.

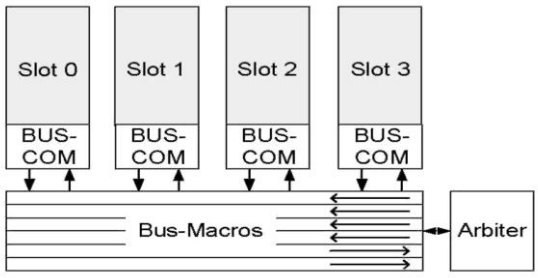


Fig: 1. BUS-COM architecture

Both approaches lack flexibility and scalability due to the presence of a single physical channel. As a matter of fact, the increasing number of cores requires a major level of contention, and this may become soon unacceptable for high-performance embedded systems; in the worst case, a Denial-of-Service (DoS) would be reached. Flexibility is further limited by the static topology of the infrastructure, i.e. the logical path between each actor is defined once for all a priori, resulting in a much lower flexibility and adaptability to communication requirements.

2. Network-Based Approaches

The implicit limitations previously described are overcome by the Network-on-Chip paradigm. The NoC approach is meant to interconnect subsystems in a multi-processors environment. However, they have also been applied in Systems-on-Chips (SoCs) architectures, as the connection scheme for different computational modules. The idea is to define a set of network elements, the *switches*, whose systematic interconnection implement the desired connectivity. To exploit full advantage of a scalable and flexible solution, packet-switching mechanism is used.

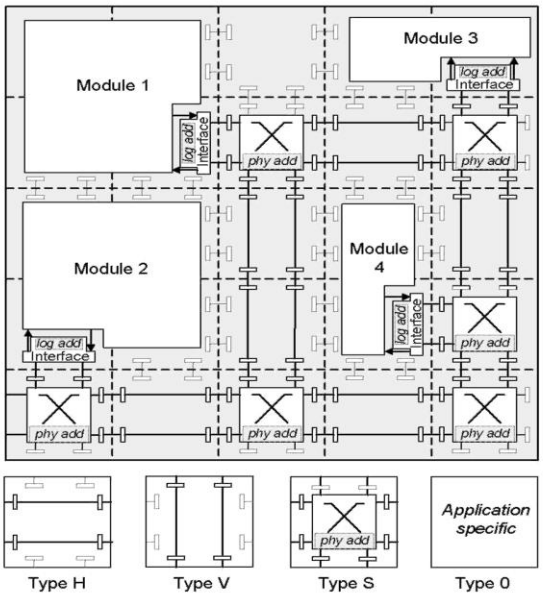


Fig: 2. CoNoChi Architecture

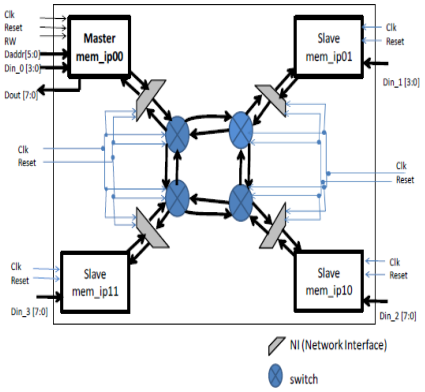
3. Existing System

This chapter gives the brief explanation about the need of the integrated architecture, advantages and applications about the proposed On-chip Communication architecture.

3.1 Need for Integrated Architecture

The work presented in related to the design and definition of a Network-on-Chip architecture tailored to dynamically reconfigurable systems. The rationale of defining such a novel communication infrastructure was the need to cope with the dynamic changes of application requirements, to achieve flexibility and adaptability, and to provide the end- user with a valid infrastructure, meanwhile taking into consideration physical resource requirements of modern FPGA devices. TheNoC architecture related to the definition of the communication protocol and the design of the elementary network node, i.e. the switch. The overall view of the work is reported in Fig. The communication side of the target system has been abstracted from the computational one, so that optimization of the two aspects can be performed independently: the Network-Interface abstracts the communication mechanisms from the computational aspect, exported by the upper-level modules. In this case, the communication level of the System-on-Chip is represented by the systematic interconnection of distributed network nodes, while the computational layer is composed of application-dependent Processing Elements (PEs) exploiting the desired logic.

Block diagram with existing method



Top level block diagram for NOC architecture

4. Proposed System

It is clear from Fig. how the communication is asymmetric; in that Master and Slave components are different (only Master-level PEs can initiate data transfer). However, this design has an implicit limitation: the NI's are *directly* attached to the corresponding core, resembling the NoC architecture interface. In this way, the design does not scale well with the increasing number of cores, since the number of NI (Network Interface) is linear with the number of PEs in the system, and this reflects on the resource requirements of the FPGA. Additionally, an increasing number of NIs demands for an increasing number of switches in the NoC, in order to ensure a minimum level of performance and connectivity. This issue has been solved in the work hereby presented. The NI design has been tailored to the on-chip bus, so that a certain number of upper-level cores can be interfaced to the NoC by means of a single NI. In this way, the scenario reported in Fig. arises, in which cores are grouped in independent communication domains, and cooperation between remote PEs can be performed by means of the shared NoC architecture.

Employing such architecture in the desired System-on-Chip is useful for several reasons:

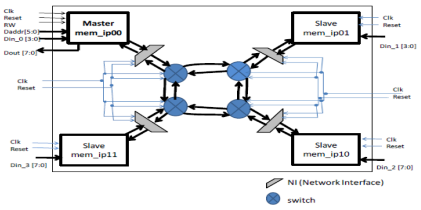
- *I*ndependent communication domains can be established in a fully transparent and flexible way.
- *D*ifferent communication mechanisms can be effectively used for different communication domains, so that design effort can be focused on computational part rather on communication details.
- *It* can extend the number of cores that can be integrated within the system, since bus-wide addresses are known only by the interfaces.
- *T*he proposed NoC approach is not meant to be used in a separate environment, but it can be truly used along with different communication paradigms, to allow true system integration.

Network on chip interconnect technology applicable to:

- Mobile phone applications processors and modem to easily connect them.
- Mobile wireless products.

- While converting total CPU design into single chip.

Block diagram with existing method



Top level block diagram for NOC architecture

5. Experimental Results

This chapter presents the Simulation and Synthesis results for the NoC and Integrated NoC with Bus architectures.For simulation and Synthesis Model Sim 6.3g_p1 and Xilinx ISE 7.112i.1 implemented using target device xc3s1600e-

5.1 Simulation: Result for Master

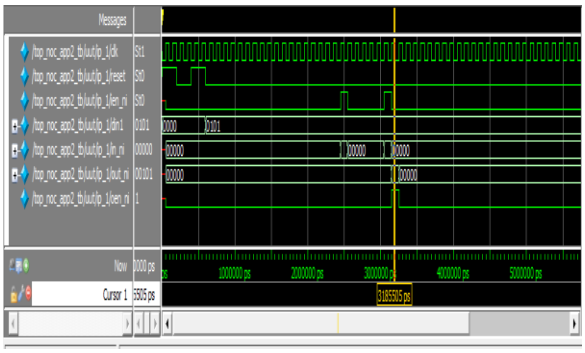


Fig: 5.

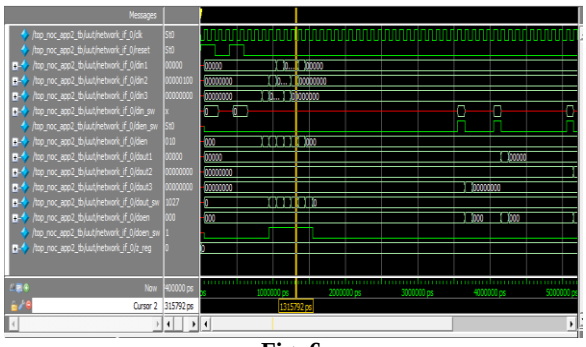


Fig: 6.

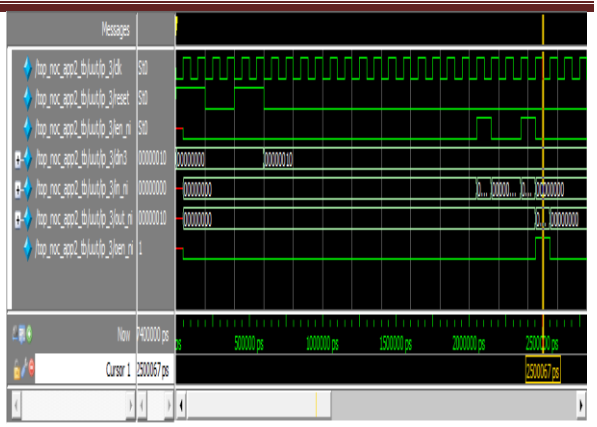


Fig: 7.

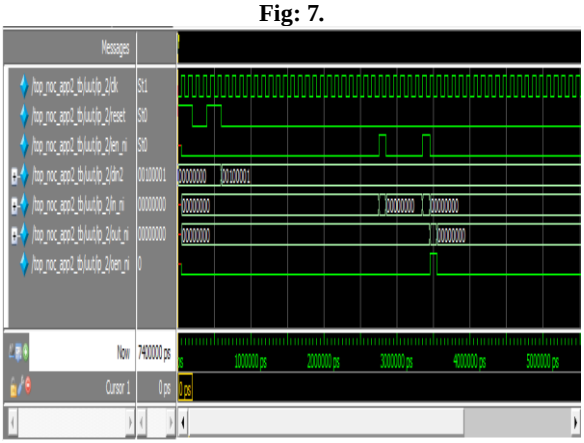


Fig: 8.

6. Conclusion

The proposed integrated NoC architecture design will make less area when compared to the existing network bus architecture which occupies less digital components. The less no of digital components makes the gate-levelcounts in less number, which leads to increase the speed of the circuit and consumes less amount of power in the soc level intergration.

7. Future Work

Integrated NoC with bus based architecture can be used for designing an (re)configuration controller which can be useful in dynamic changing environment ,where the real communication requirements cannot be know in advance, before the real application execution.

References

[1] S. Borkar, Thousand core chips—A technology perspective, in Proc.ACM/IEEE Design Autom. Conf. (DAC), 2007, 746–749.

[2] P.-H. Pham, P. Mau, C. Kim, A 64-PE folded-torus intra-chip communication fabric for guaranteed throughput in network-on-chip based applications, in Proc. IEEE Custom Integr. Circuits Conf.(CICC), 2009, 645–648

[3] C. Neeb, M. J. Thul, N. Wehn, Network-on-chip-centric approach to interleaving in high throughput channel decoders, in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2005, 1766–1769

[4] H. Moussa, A. Baghdadi, M. Jezequel, Binary de Bruijn on-chip network for a flexible multiprocessor LDPC decoder, inProc.ACM/IEEE Design Autom. Conf. (DAC), 2008, 429–434

[5] V. E. Beneš, Mathematical Theory of Connecting Networks and Telephone Traffi, New York: Academic Press, 1965