Performance Evaluation of Nine-Level Modified Cascaded Symmetric Inverters with Different PWM Techniques

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Article Info
Article history:
Received 3 February 2015
Received in revised form
20 February 2015
Accepted 28 February 2015
Available online 6 March 2015

Keywords
Modified MLI,
MCPWM,
Symmetric Topology,
Single PWM,
THD

Abstract
Multilevel inverters are extensively used in flexible power systems because of their high quality and near sinusoidal output with low harmonic distortion level. The quality of output voltage depends on the number of output levels. In this paper, two different approaches in symmetric multilevel inverter with lessened number of switches are proposed. The first topology uses sub multilevel cells connected in cascade. The second approaches only single H-bridge and uses two techniques. One is the PWM technique with multiple carriers and another one is the single PWM method. The simulation results with MATLAB/ Simulink are presented for nine level modified inverters and the comparison has been made based on some factors such as number of switching devices and the total harmonic distortion for different values of loads. The hardware of the topology presented has been also implemented and the results has been analysed.

1. Introduction

Multilevel Inverter, a device used to synthesise the output AC voltage from the multiple DC Sources. The output has the specified count of voltage levels based on either the count of input voltage sources or the count of switches used [1, 2]. The multilevel inverters have been proposed for low and medium power applications in the recent years because of their high quality in output power and low harmonic distortion [3]. The concept of multilevel inverter is divided in to two groups, with single input source and with multiple input sources. Flying capacitor inverter and Diode clamped inverter or neutral point clamped have single voltage source and the count of output voltage levels are equal to the switches used in the circuit [4]. The predominant disadvantage in the diode clamped inverter is the problem in real power flow because of the DC levels overcharge without the precise control of diodes. The predominant disadvantage of flying capacitor multilevel inverter is the balancing of voltage levels in all the capacitors [6] and it requires additional precharging circuitry [7]. The efficiency is not satisfactory and the performance in the low modulation index is also poor [8]. Packaging is also difficult due to the large amount of capacitor banks [9-11].

Cascaded multilevel inverter is the other type has multiple input voltage sources and the output voltage levels are based on the sources. This type of inverter is called as the true inverter because the output voltage is derived from the various input voltage sources and useful for the renewable energy source applications [12]. If the values of all input sources are equal, then the topology is called as the symmetric topology otherwise it is called as the asymmetric topology. In this paper, concept of cascaded multilevel inverter has been taken and the drawbacks of the inverter are considered.

The nine level cascaded inverter (CHB) is depicted in fig.1 for which the output voltage levels have the following relationship with the number of input DC sources.

Let N is the number of independent DC sources used, then the number of voltage levels = 2N+1, and the number of switches = 4N.

The predominant disadvantage of this inverter is the amount of switches used in each level is high compared to other inverters. To reduce this count, new types of multilevel inverters have been used.

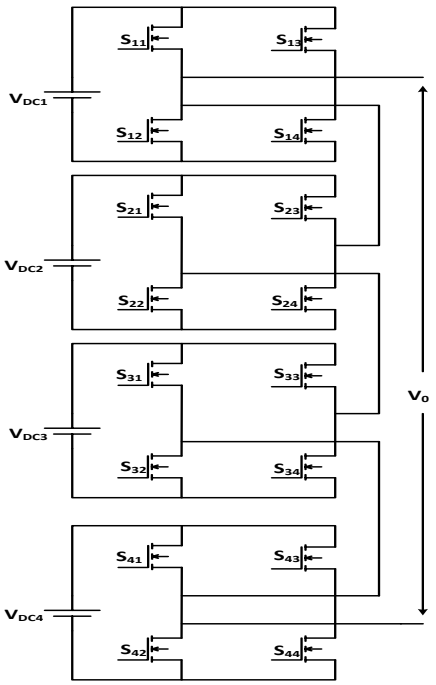

Fig: 1. Cascaded nine-level Inverter

In this paper, two new topologies have been presented and analysed. First topology uses sub multilevel cells with H-Bridge in each cell to produce required output level and the Second topology uses cascaded voltage sources with Single H-Bridge. For the detailed analysis of harmonics,

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two PWM pulse generation methods have been used in the second topology. First one is using multiple carriers for a single sine wave reference (MSPWM) and the next one is Single PWM method.

2. Modified Nine-Level Inverter

(i) Sub Multilevel Cell Topology

A sub multilevel cell consists of N number of independent DC voltage sources which are used to produce a multilevel voltage output by using power electronic switches [2]. In one sub cell we can connect many voltage sources upto the voltage rating of the switches S_{1M} - S_{4M}. M will be the number of sub multilevel cells connected in cascade. The general structure of the inverter is given in fig.2 and the nine-level inverter is depicted in fig.3.

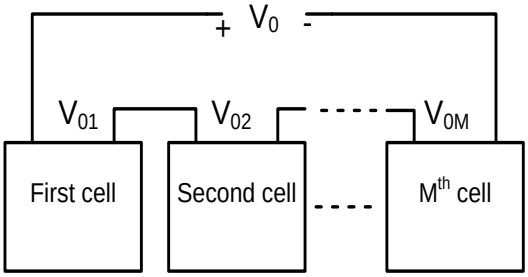


Fig: 2. General Structure of Sub Multilevel Cell Inverter

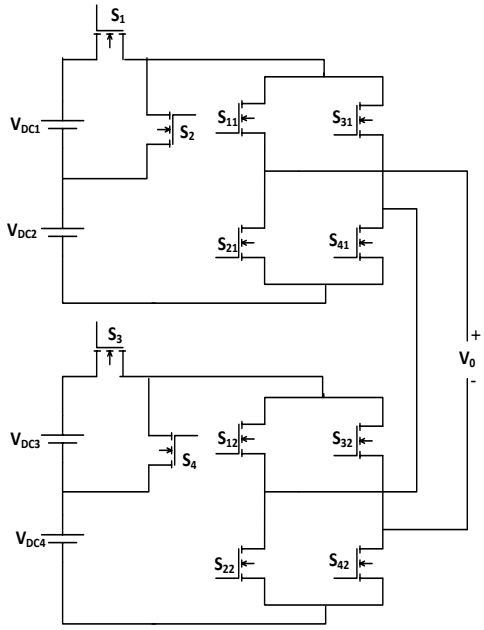


Fig: 3. Nine-level Inverter with two sub Cells

The output voltage levels are defined by the number of sovereign DC sources (N) and the number of sub multilevel cells (M).The total number of switches used in the circuit is defined by the number of sovereign DC sourced used in the circuit.

Number of output voltage levels = *2MN+1*
Number of switches = *2M(N+1)*
Number of H-Bridges = *M*
Maximum output voltage = MNV_{DC} if VDC1 = V_{DC2}=…. = V_{DC}

For a nine level inverter, two sub multilevel cells have two voltage sources each are cascaded. Twelve switches are used to get the prescribed output. There are so many switching combinations to achieve the staircase output. The relationship between the number of levels and switching combinations is given by [5]:
Number of switching combinations = 2^{N-1}

(ii) Single H-Bridge Topology

Modified nine-level inverter with single H-Bridge that depicted in fig.4 requires less switches compared to the conventional nine-level inverter and sub multilevel cell based inverter. The modified inverter for which the output voltage levels have the following relationship with the number of input DC sources.
Let N is the number of independent DC sources used,
Then the number of voltage levels = 2N+1
The number of switches = N+4.
Number of diodes = N-1.
If VDC1 = VDC2 = VDC3 = VDC4 = + Vdc,

Then the overall output changes from +4 VDC to –4Vdc.For a nine level inverter only 8 switches and 3 diodes are required compared to 16 of conventional inverter and 12 of sub multilevel cell inverter.

Table: 1. Switching Sequence of nine-level Inverter

Duration	ON Switches	ON Diodes	Voltage Levels
Positive Half Cycle (S_{11}& S_{41} ON)	-	D_1, D_2, D_3	0
	S_3	D_1, D_2, D_3	+ V_{DC}
	S_3, S_4	D_1, D_2	+2 V_{DC}
	S_2, S_3, S_4	D_1	+3 V_{DC}
	S_1, S_2, S_3, S_4	-	+4 V_{DC}
Negative Half Cycle (S_{21}& S_{31} ON)	-	D_1, D_2, D_3	0
	S_3	D_1, D_2, D_3	-V_{DC}
	S_3, S_4	D_1, D_2	-2 V_{DC}
	S_2, S_3, S_4	D_1	-3 V_{DC}
	S_1, S_2, S_3, S_4	-	-4 V_{DC}

The losses due to switching are also reduced. This type of inverter consists of a conversion unit with a switching device connected in series with a Voltage source and a diode. The number of conversion units is equal to the count of output levels. For a nine level inverter, four conversion units are cascaded and connected to an H-Bridge Inverter. By triggering S_3, VDC3 is obtained at output which is equal to Vdc. Similarly, by triggering S_3 and S_4, we can obtain the output voltage as the addition of VDC3 and VDC4 equal to +2Vdc. If all the switches (S_1, S_2, S_3 and S_4) are ON, the +4Vdc level is obtained. The switching sequence of nine-level inverter is given in table.1. and the output wave form generation is shown Fig.5.

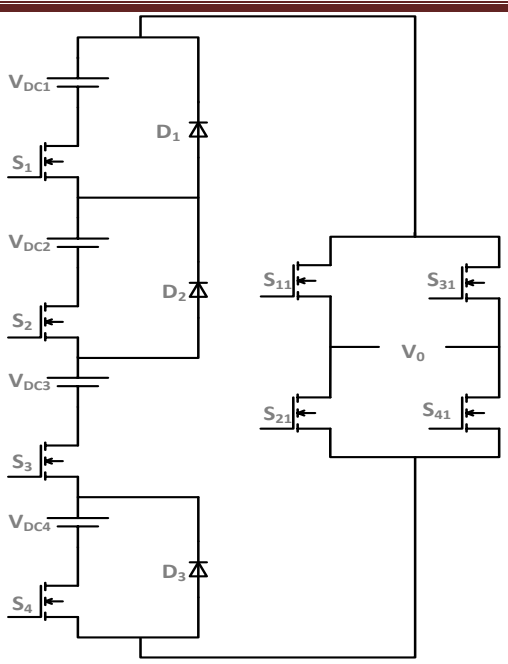


Fig: 4. Modified Nine Level Inverter

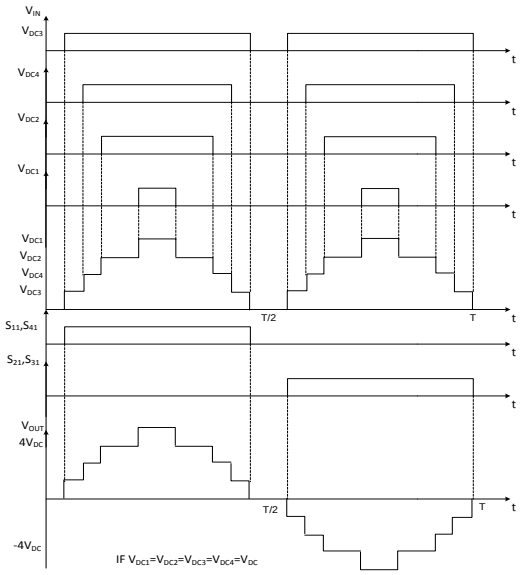


Fig: 5. Output waveform of nine-level Single H-Bridge Inverter

The output levels are unidirectional. By using H-Bridge the output is converted into bidirectional. The output waveform of the H-Bridge contains nine levels as depicted in fig.3. At positive half cycle, Switches S_{11} and S_{41} are on and during negative half cycle S_{21} and S_{31} are on in the H-Bridge inverter.

3. PWM Techniques

(i) MCPWM Technique

In the Multiple carrier PWM (MCPWM) method, (m-1) carrier signals with same frequency f_c and Amplitude A_c are compared with a reference sinusoidal waveform of amplitude A_r and frequency f_r. The frequency of the reference signal determines the frequency of the output waveform which is shown in fig.6.

In MCPWM technique, the modulation index of Amplitude modulation M_{am} and the modulation index of frequency M_{fm} are defined as

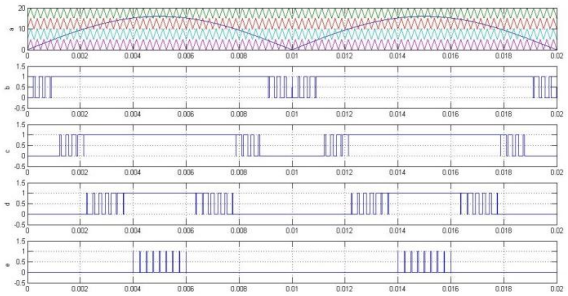


Fig: 6. Generation of Switching Waveforms using MCPWM Technique

$$M_{am} = \frac{2A_r}{(m-1)A_c}$$

$$M_{fm} = \frac{f_c}{f_r}$$

To reduce harmonics, the maximum value of frequency modulation index will be not more than 30 ($M_{fm} \leq 30$). For a normal 50 Hz reference signal, the carrier frequency is not more than 1.5 KHz.

(ii) Single PWM Method

In this method, a sinusoidal reference signal with the frequency equal to the output frequency is compared with four different DC voltage levels. The pulses are generated according to the values of the DC voltages compared. Normally, in single PWM, carrier will be a triangular waveform or Ramp waveform. But, in this paper, a sine waveform is compared with a square waveform to get the output nearly a sinusoidal waveform shown in fig.7 and fig.8.

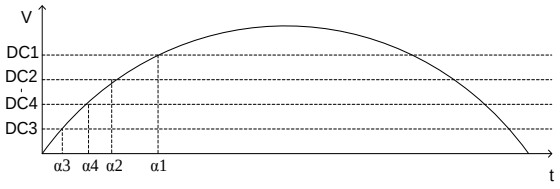


Fig: 7. Generation of Firing Angles using single PWM Method

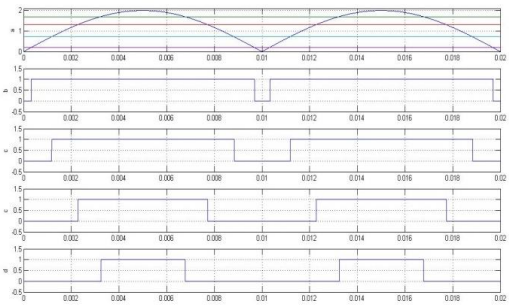


Fig: 8. Generation of switching waveforms using Single PWM Method

To minimize the harmonics in the multilevel inverter, the firing angles of various stages can be selected accordingly. Newton Raphson method is optimal for the firing angle selection [12]. For a nine level inverter, four firing angles α1, α2, α3 and α4 can be selected at different values in order to reduce the lower order harmonics. The conditions to select the firing angles are given by the following

$\alpha 3 < \alpha 4 < \alpha 2 < \alpha 1 < 90^{o}$

$\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3) + \cos(\alpha 4) = (m-1) * M/2$

where M – modulation index and

m – Number of output levels.

And the modulation index M is

$$M = \frac{2V_{c\,(peak)}}{(m-1)V_{dc}}$$

Vc(peak) – Peak Carrier Voltage, m – Number of output levels for the given nine-level inverter, we have chosen the M value as 0.9 for effective harmonic elimination. Hence, equation (2) can be rewritten as,

$\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3) + \cos(\alpha 4) = 8*0.45 = 3.6$

The value of α1, α2, α3 and α4 was selected to satisfy the above condition.

After calculating the firing angles, we can find the value of DC voltages by applying the following equation.

$DC_i = \sin(\alpha_i)$ where i=1,2,….n

Similarly, the value of DC2, DC3 and DC4 arecalculated to satisfy the above conditions of newton Raphson method

4. Simulation Results –Analysis

The simulation models of multilevel inverters have been developed using SIMULINK of MATLAB. Pulse generation scheme for the two methods are depicted in fig.9 and fig.10. Different combinations of RL loads are used to calculate the total harmonic distortion. Fig.11. shows the output voltage of the inverter with sub multilevel cells. The output of MCPWM Inverter is shown in fig.12 and single PWM inverter is depicted in fig.13. The circuits are designed to produce an output voltage of 200V as per the maximum voltage level calculation of the circuit. As the figures show, the circuit generates the expected output voltage levels resulting in the 9-level load voltage.

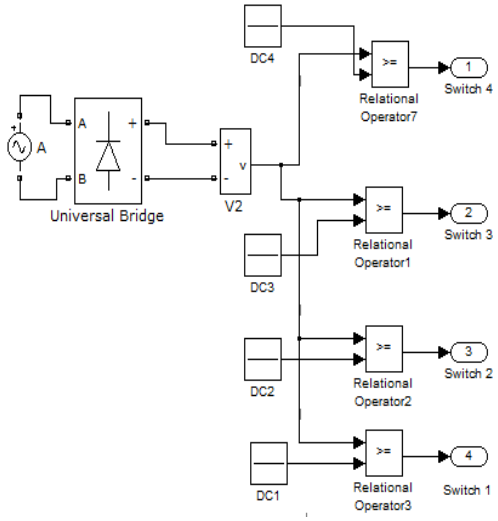


Fig: 9. Pulse Generation Scheme using Single PWM Technique

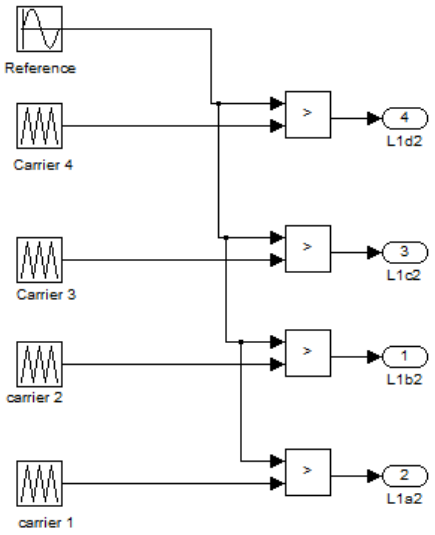


Fig: 10. Pulse Generation Scheme using MCPWM Technique

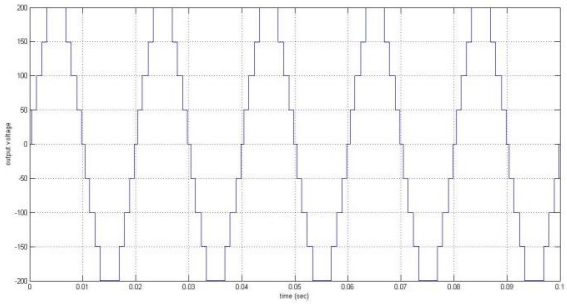


Fig: 11. Output Voltage waveform of Sub Multilevel cell MLI

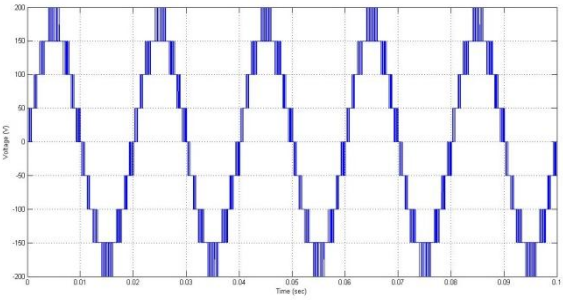


Fig: 12. Output Voltage Waveform of MCPWM MLI

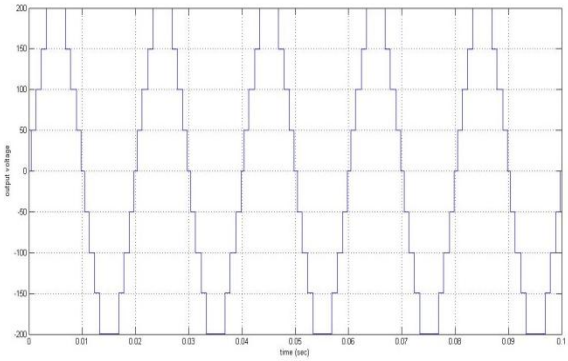


Fig: 13. Output Voltage Waveform of Single PWM MLI

The choice of the inverter should be made between the total harmonic distortion and the number of switches. The Total Harmonic Distortion (THD) has been calculated for the MLI's. All these values are calculated for the modulation index of reference signal as 0.9. Table 2 shows the THD comparison with the number of switches required also. Since the harmonic values of SHB by using MCPWM is around 5% at all load conditions, the circuit is analysed by giving the pulses at different modulation index values range from 0.7 to 1.1 and the THD values were analysed. Table 3 shows the THD comparison of single H-Bridge inverter using MCPWM with different modulation indexes. Fig.14.shows the graphical representation of the comparison of THD values calculated for the different modulation indexes. With all the calculated values, comparison has been made on the harmonic values of three types of inverters presented. Fig.15 shows the graphical representation of minimum THD values calculated for three types of inverters.

Table: 2. Minimum THD Values of MLI

Type of inverter / switching technique	Number of switches	Minimum THD (%) with various RL loads		
		400 Ω / 10mH	200 Ω / 10mH	100 Ω / 10mH
Sub Multilevel cell topology Inverter with Single PWM	12	9.63	9.36	9.29
SHB with Single PWM	8	9.64	9.62	9.15
SHB with MCPWM	8	4.44	4.47	4.72

Table: 3. THD Values of MCPWM at Different Modulation Indexes

Modulation Index	400 Ω / 10mH	200 Ω / 10mH	100 Ω / 10mH
0.7	6.47	6.49	6.64
0.8	5.58	5.6	5.75
0.9	**4.44**	**4.47**	**4.72**
1	5.07	5.1	5.32
1.1	5.2	5.22	5.43

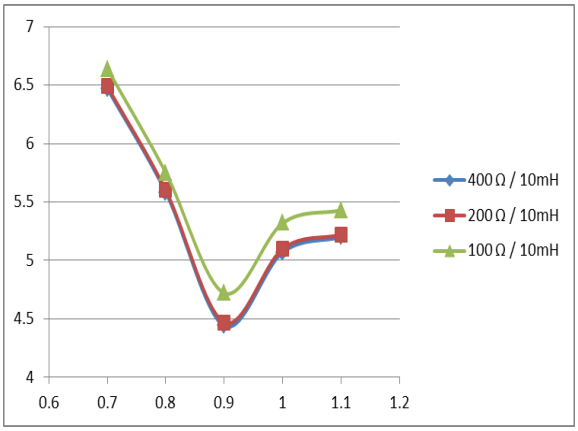
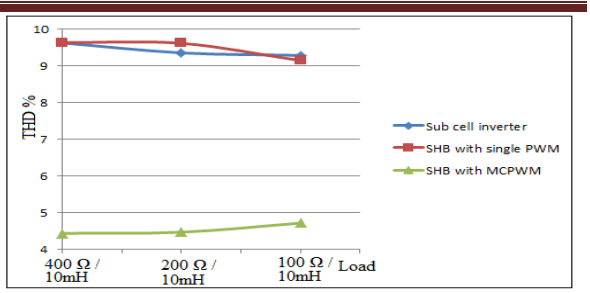


Fig: 14. Comparison of THD Values of MCPWM at Different Modulation Indexes



Fig; 15. Comparison of THD Values for Different Types of Inverters

5. Hardware and Result

To prove the simulation results, the hardware of the Single H-Beridge inverter shown in fig.16 has been implementaed. AlteraCyclone VLSI kit has been used and the IRF640 MOSFET is used as switch. The pulses for the MOSFET IRF640 have been generated using VLSI kit and the performance of the inverter has been analysed and the results are given in fig.17.

6. Conclusion

The modified multilevel inverters with reduced number of switches have been presented in this paper. Since the THD value is nearly equal, the single H-Bridge topology uses only 8 switches for the same output which is two third of that of the sub multi-level cell topology (12 switches). By using two pulse generation techniques, the performance of the single H-Bridge topology has been analysed. Since the Single PWM method reduces the complexity in the pulse generation circuit but MCPWM technique reduces the total harmonic distortion on the circuit and power factor also improved. Hence, the Single H-Bridge inverter with MCPWM method is suitable because of the number of switches and THD

Fig: 16. Hardware Implementation of Single H Bridge MLI

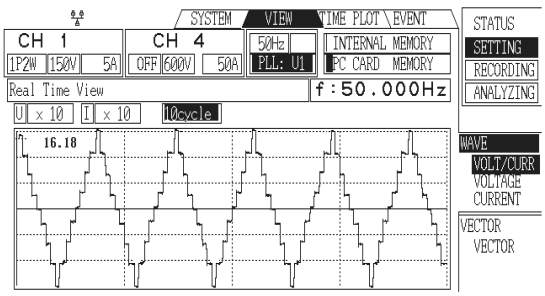


Fig: 16. Output Voltage Waveform of Single H Bridge MLI

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