High Performance NOC Router Design

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Abstract
In this paper, accurate localizations of the faulty parts of the NoC are handled. An error detection mechanism suitable for dynamic NoCs, is used to find faulty blocks or processing element where the number and position of processor elements or faulty blocks change with an increase in size of network. An adaptive routing algorithm is used in this paper. Both error detection mechanisms and routing algorithm are able to distinguish permanent and transient errors and localize accurately the position of the faulty blocks (data bus, input port, output port) in the NoC routers. It maintain throughput, the network load, and the data packet latency. We provide localization capacity analysis of the presented mechanisms, NoC performance evaluations, and field-programmable gate array synthesis.

1. Introduction

To meet the growing computation intensive applications and the needs of low-power, high performance systems, the number of computing resources in single-chip has enormously increased, because current VLSI technology can support such an extensive integration of transistors. By adding many computing resources such as CPU, DSP, specific IPs, etc to build a system in System-on-Chip, its interconnection between each other becomes another challenging issue. In most System-on-Chip applications, a shared bus interconnection which needs bus access requests, to communicate with each integrated processing unit because of its low-cost and simple control characteristics. However, such shared bus interconnection has some limitation in its scalability because only one master at a time can utilize the bus which means all the bus accesses should be serialized by the arbitrator. Therefore, in such an environment where the number of bus requesters is large and their required bandwidth for interconnection is more than the current bus. Bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from traditional large-scale multi-processors and distributed computing networks. The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. The main problems of using buses are Power, size and performances are not practical for multi-processor chips using a single bus interconnection. And the solution for this is using Network on chip (NoC), which is based on interconnection that provide fast, reliable data and low power consumption. The NoC architecture is characterized by the number of routers which is linked to processing elements in the array, the bandwidth of the communication channels between the routers, the topology of the network and the mechanism used in data transmission.

The topology of the network is defined through the arrangement of routers and processor connection on the device. The most commonly used topology is the 2-D mesh topology, which looks like an arrangement of tiles as shown in Fig.1.

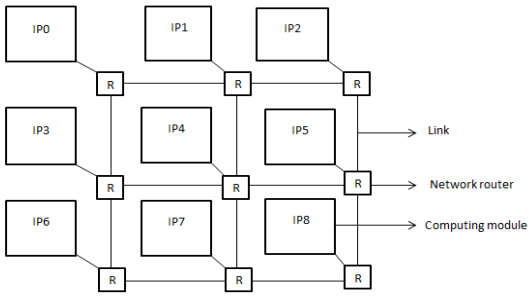

Fig: 1. Network on Chip

2. Proposed Router Architecture

A new reliable NoC-based communication approach called RKT-NoC. The RKT-NoC is a packet switched network based on intelligent independent reliable router called RKT-switches. The RKT-switch is characterized by its architecture having four directions (North, South, East, and West) suitable for a 2-D mesh NoC. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP. The proposed detection mechanisms can also be applied to NoCs using five-port routers with a local port dedicated to an IP. However, the major drawback of these architectures is when the local port has a permanent error and the IP connected to it is lost or needs to be dynamically moved in the chip because of the dynamic partial reconfiguration. The four-port RKT-NoC, an IP can replace several routers by having several input ports and hence be strongly connected in the network. Moreover by using dynamic partial reconfiguration and IPs strongly connected in the NoC, no one fault location is more catastrophic than another. Indeed, an IP may have access to the network by being connected to several routers, or can be dynamically moved on the chip if this only access point becomes faulty. Each port direction is composed of two unidirectional data buses (input and output ports). Each input port is associated to a first-input, first-

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output (FIFO) (buffer) and a routing logic block. The RKT-switch operation is based on the store and forward switching technique. This technique is suitable for dynamically reconfigurable NoCs. At any instant with the store and forward technique, each data packet is stored only in a single router. Hence, when a router needs to be reconfigured, the. router is only required to empty its buffers. With the wormhole switching technique, a single data packet can be spread over several routers. Consequently, the time required to clear all the routers containing partial packet data (flits) and to reconstruct these packets before performing a reconfiguration is more significant. The RKT-NoC uses no bouncing routers, so that if a router is surrounded by three unavailable neighbors, it also becomes unavailable.

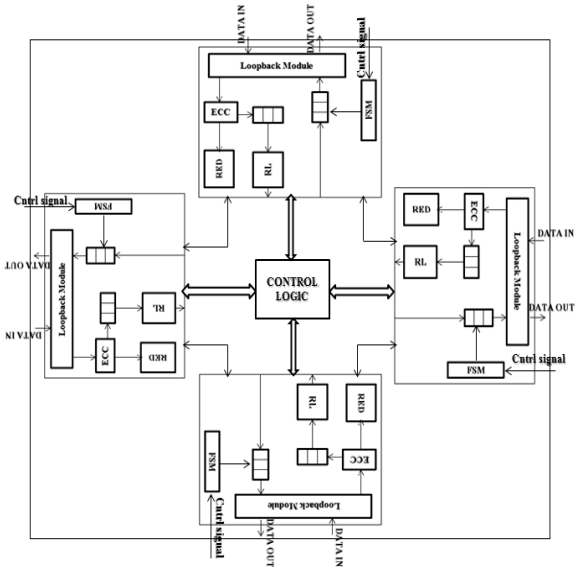

Fig: 2. Proposed Router Architecture

Indeed, if a data packet is sent to a router surrounded by three unavailable nodes, the packet cannot be routed. The data flow control used in the architecture is the Ack/Nack solution, which can handle fault-tolerant transmission, although this does increase the energy consumption. This solution relies on the retransmission of packets being received as faulty by a neighboring node. Being able to perform a packet retransmission after it has been sent to a node requires that a copy of the packet be locally saved until an Ack or Nack is received. If a neighboring router receives a flit containing an error that cannot be corrected by the ECC, a Nack is sent back and the whole packet is retransmitted. Otherwise an Ack is generated at full packet reception. More precisely, an Ack is generated only when all the flits of the data packet have been received and checked by the router, which reduces latency. The Hamming ECC is considered in order to provide a convenient tradeoff between area overhead and error correction capacity.

Fig: 3. Architecture Flow

This choice permits the correction of single event upset (SEU) errors (one bit flip in a flit) and the detection of multiple event upset (MEU) errors (two bit flips in a flit).The Hamming code is more suitable for NoCs based on Ack/Nack flow control than the parity bit check. Indeed, on a single bit-flip error occurrence, error correction is possible with the Hamming ECC, whereas the single parity check would require packet retransmission and hence an increased transmission latency.

A. Routing Logic

Routing acts as the backbone to avoid deadlock and live lock. The routers have the address in the matrix format i.e., it is defined by its xy coordinated. Fig. 3.3 show the router structure in which input packet or data packet enters the packet detection module. If the input trigger is one means the incoming packet will go to two modules. One is decision making module and another one is incoming packet storage. The decision making module will decide the direction of the data packet in which direction the data packet should be move.

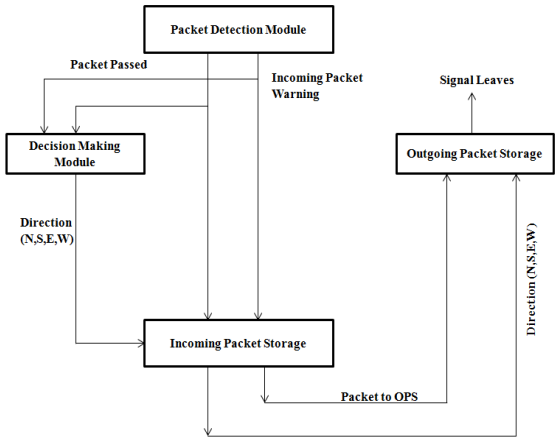

Fig: 4. Decision Making Module

Incoming packet storage is used to receive both the direction of the packet that is whether the packet should move to north, south, east or west and the header of the incoming packet. Both directions of the data packet and the header of the incoming packet are forwarded to the outgoing packet storage.

B. Error Correction

Transmission of data without any error in the Network on Chip ensures integrity of data. To guarantee error free transmission of messages, the error correcting techniques is included in the switch to avoid both routing error and data error. This paper uses cyclic redundancy for data error checking, which has the tendency to check burst errors. If error occurs then it sends a negative acknowledgement to the source requesting for retransmission. Each switch is identified by a unique address mentioned in matrix form. When a message is passed from one IP core to another IP core via switch, it checks the status of the flits received. Flits received through the loop back mechanism indicate that the router ahead is faulty. The flits routed by XY algorithm states that the router ahead is not faulty. If adaptive XY algorithm is used then the flits are received to bypass the faulty router. The availability of the next router

is determined by checking the status of the availability signal along the diagonal direction. Thus the routing error detection mechanism is highly suitable to avoid both dead lock and live lock, Deadlock is a situation that occurs when a packet is waiting for an event that can never happen because of circular dependence on resources. Livelock, on the other hand, is a configuration of the network in which packets continue to move, but never reach their destination.

3. Simulation Results

The simulation for routing logic is done using Modelsim simulator.

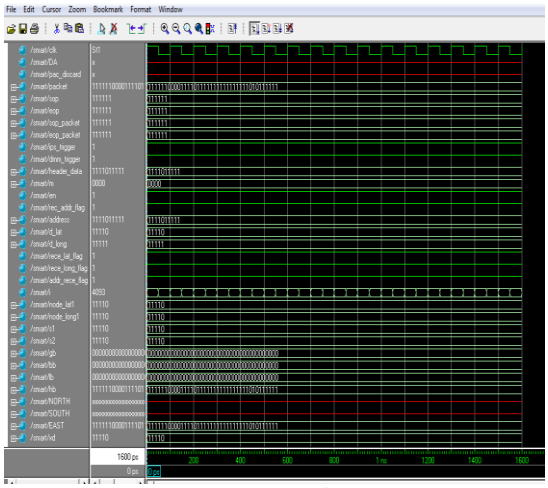

Fig: 5. Simulation Result for Router Logic

3.1 Synthesis Result

The schematic view and power analysis can be obtained by synthesizing in Xilinx software. The IC view is shown in fig 4.4.

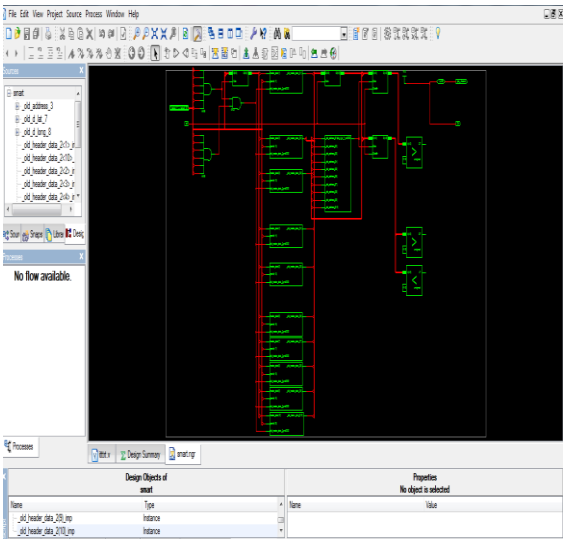

Fig: 6. RTL Schematic

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

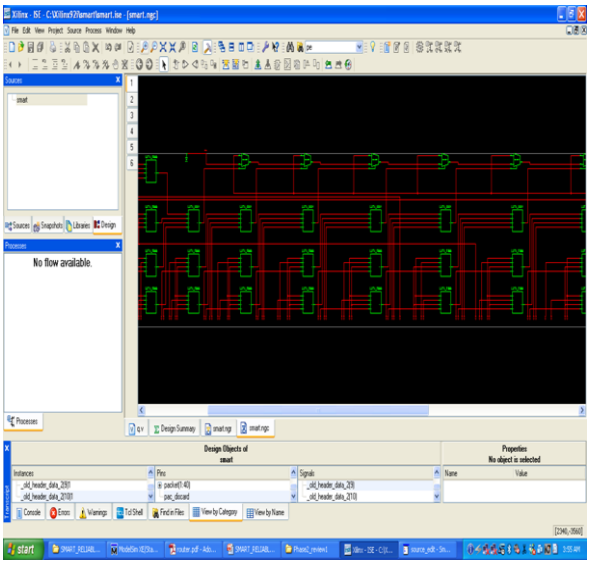

Fig: 7. Technology Schematic

Viewing a Technology schematic opens an NGC file that can be viewed as an architecture-specific schematic. This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of of LUTs, carry logic, I/O buffers, and other technology-specific components.

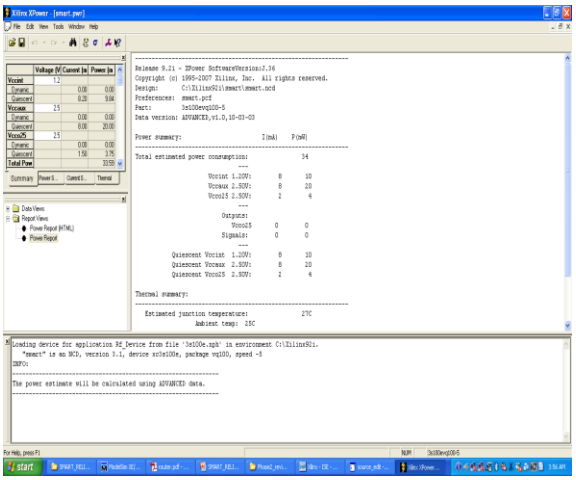

Fig: 8. Power Analysis

4. Conclusion

The proposed router architecture in this paper includes an advanced routing logic and burst error correction mechanism. So it is well suited for the network under heavy traffic conditions. Increasing the number of intellectual properties increase the traffic and this router connection in NoC will be useful to detect and correct the errors. This switch also gives a better solution to avoid deadlock and live lock conditions. This switch can be analyzed for various traffic conditions and the performance can be evaluated for the entire network architecture.

References

[1] K. Sekar, K. Lahiri, A. Raghunathan, S. Dey, Dynamically configurable bus topologies for high-performance on-chip communication, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 16(10), 2008, 1413–1426

[2] G.-M. Chiu, The odd-even turn model for adaptive routing, IEEE Trans. Parallel Distrib. Syst., 11(7), 2000, 729–738

[3] C. Grecu, A. Ivanov, R. Saleh, E. Sogomonyan, P. Pande, On-line fault detection and location for NoC interconnects, 12th IEEE Int. On-Line Test. Symp., 2006, 145–150

[4] M. Hosseinabady, M. Kakoee, J. Mathew, D. Pradhan, Low latency and energy efficient scalable architecture for massive NoCs using generalized de Bruijn graph, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 19(8), 2011, 1469–1480

[5] S. Jovanovic, C. Tanougast, S. Weber, C. Bobda, A new deadlock-free fault-tolerant routing algorithm for NoC interconnections, Int. Conf. Field Program. Logic Appl., 2009, 326–331

[6] D. Park, C. Nicopoulos, J. Kim, N. Vijaykrishnan, C. Das, Exploringfault-tolerant network-on-chip architectures, Int. Conf. Depend. Syst. Netw., 2006, 93–104

[7] J. Raik, V. Govind, and R. Ubar, An external test approach for network-on-a-chip switches, 15th Asian Test Symp., 2006, 437–442

[8] A. Pullini, A. Federico, D. Bertozzi, L. Benini, Fault tolerance overhead in network-on-chip flow control schemes, 18th Symp. Integr. Circuits Syst. Design Conf., 2005, 224–229

[9] T. Pionteck, R. Koch, C. Albrecht, Applying partial reconfiguration to networks-on-chip, Field Program. Logic Appl. Int. Conf., 2006, 1–6

[10] S. Jovanovic, C. Tanougast, C. Bobda, S. Weber, CuNoC: A dynamic scalable communication structure for dynamically reconfigurable FPGAs, Microprocess. Microsyst., 33(1), 2009, 24–36