Guaranteed Multicast Scheduling in All Optical Interconnects

C. Subashree [a], N. Mary Helen [b]

[a] Department of M.E-communication system, Mookambigai College of Engineering, Pudukkottai, Tamil Nadu, India

[b] Department of Electronics and Communication Engineering, Mookambigai College of Engineering, Pudukkottai, Tamil Nadu, India

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Abstract

Optical interconnects are considered as a very appealing solution for high-throughput, energy-efficient and transparent packet forwarding in core networks and parallel computers. We first propose a novel optical buffer called Shared-enabled fiber-delay lines (S-FDLs), which can provide flexible delay for copies of multicast packets using only a small number of FDL segments. We then present a Guaranteed Multicast Scheduling (GMS) Algorithm that considers the schedule of each arriving packet for multiple time slots. The performance of GMS is evaluated extensively against statistical traffic models and real Internet traffic traces, and the results show that the proposed GMS algorithm can achieve superior performance in terms of average packet delay and packet drop ratio.

1. Introduction

Optical networking has been wide adopted to move high volume traffic in backbone networks thanks to the massive bandwidth of optics. All-optical packet switches ar thought-about as a awfully appealing answer for high-throughput, energy efficient and clear forwarding in backbone networks. During the past few years, as driven by the increasing multicast applications requiring high-bandwidth transmission from one source to multiple destinations, like video conference, video-on-demand (VoD) and IP-based tv (IPTV)], optical multicast packet shift has attracted a lot of research effort. A series of all-optical shift architectures and technologies are planned to support multicast at the switch/router level, like wavelength-assisted shift, Broadcast-and-Select (BS) shift, etc. Despite of the sizeable quantity of labor on multicast capable optical packet shift architectures, however, relatively little attention has been paid on multicast planning in such switches, that is vital for high-speed all-optical packet switches. motivated by this observation, during this paper we contemplate multicast planning in optical packet switches. A major challenge for multicast planning in optical packet switches is that the resolution of output rivalry, which occurs once multiple optical packets at the same time head to the same output. Specifically, the very fact that multicast packets usually have quite one destination outputs intensifies output rivalry. Since a sensible "optical RAM" ready to mimic the buffers utilized in electronic switches continues to be not obtainable currently, numerous rivalry resolution techniques have

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Corresponding Author,
E-mail address: c.subashreeece@gmail.com

and CCF-0915495 been planned. Buffer-less approaches like wavelength conversion and deflection routing [5] resolve contentions by sending conflicted packets to totally different wavelengths or different outputs. However, they need been shown to be ineffective for avoiding packet loss beneath full network conditions and demand plenty of network resources. Electronic buffers have been thought-about to be utilized in Ops, making "hybrid" electronic/optical switches [6]. However such associate approach requires Optical-to-Electronic-to-Optical (OEO) conversion, which results in undesirable power consumption and extra cost in high speed shift. On the opposite hand, fiber-delaylines (FDLs), a passive device ready to delay optical packets for a set amount of your time, give a sensible resolution for output rivalry in Ops, thanks to its transparency to traffic bit-rate and low power dissipation. Multicast planning in optical packet switches with FDLs buffer is considerably totally different from the well-studied multicast scheduling in electronic switches [10],for the explanation that all the approaches for electronic switches place confidence in electronic RAM to resolve output rivalry, whereas FDLs will simply delay packets for a set amount of your time. many multicast\ scheduling schemes victimisation FDLs as buffer are planned [4]. Among them, a wide adopted theme is output buffering [12], within which associate output buffer consisting of an N ×B switch associated B FDL segments with fastened progressive delay is placed at every output. Throughout every planning cycle, the hardware assigns a FDL phase with correct delay in every output buffer to the packets destined for that output. To achieve a reasonable packet ratio and network link utilization, the output buffering theme needs an oversized quantity of FDL segments to construct output buffers. Since FDLs ar large, such associate approach isn't scalable for big switches. Another commonly used multicast planning theme is wavelength assisted routing [4], [13], within which multicast packets are sent to multicast modules, a FDL loop device wont to generate copies of the packet and supply necessary delay. However, wavelength-assisted routing will give solely restricted multicasting ability and its performance deteriorates quickly beneath congested traffic conditions, as every multicast module cannot be shared by multiple packets at the same time.

Moreover, wavelength-assisted routing cannot give delay guarantee since a packet might ought to be recalculated for several times in the multicast module before being sent out.

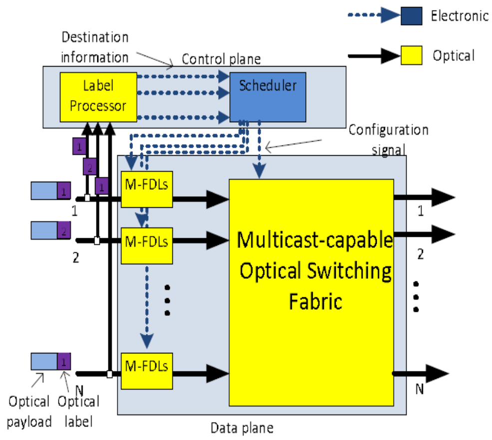

Fig: 1. The Architecture of a Single-Wavelength, input-Buffered N×N Optical Multicast Packet Switch

In this paper, we have a tendency to propose a Delay-Guaranteed Multicast Scheduling (DGMS) rule for all-optical packet switches with FDLs buffer. So as to with efficiency utilize FDLs, we also present a unique optical buffer referred to as multicast-enabled FDLs (M-FDLs) that gives versatile delay for multicast packets by victimization solely satiny low range of FDLs. the most options of the planned DGMS will be summarized as follows.

- Secure delay edge for all transmitted packets. By considering the schedule of every inward packet for multiple time slots, DGMS permits a lot of economical packet transmission than programming algorithms that resolve output competition for one interval. When network is extremely engorged, DGMS may also like a shot detect it and promptly drop packets with overlong delay to let higher layer protocols quickly reply to the network condition. Overall, we tend to show that DGMS is ready to guarantee a set delay edge for all transmitted packets no matter path, whereas keeping packet drops at a minimum level even below the foremost engorged network condition. Such a feature is particularly fascinating in delay-sensitive multicast applications, like video conferences and IPTV.
- change pipelined programming and straightforward hardware implementation. DGMS will be pipelined to cut back time complexity. Additionally, bound procedures in DGMS will be enforced by straightforward combinatorial logic circuits to further relax the temporal arrangement constraints.
- Economical buffer management. Through in depth simulations, we demonstrate that with solely atiny low variety of FDLs, DGMS can do ultra-low average packet delay with stripped packet loss below varied traffic conditions. The reminder of the paper is organized as follows. Section II present related work III presents the architecture of the adopted optical multicast packet switch and optical buffer.

2. Related Work

Switches Hao Yu, Sarah Ruepp, Michael S. Berger propose the multi-level round-robin multicast planning algorithmic rule with the look-ahead mechanism provides a extremely ascendible design and is in a position to cut back the head-offline interference downside that the weight-based algorithmic rule suffers from. Investment the Filter & Merge theme, multicast and Unicast traffic ar severally regular supported their requests. selections ar integrated following a selected policy. Remainder is coiled back to the filtering module that filters out the conflicting requests to confirm fairness. Simulation results show that comparison with the theme victimization WBA for the multicast scheduling; the theme projected during this paper reduces the HOL interference downside for multicast traffic and provides a big improvement in terms of latency. Rather than distribution a separate queue to every combination of N destinations, solely N queues ar allotted for every input port. Up to N address tokens ar generated for every inward cell, every of that is hold on within the queue akin to a destination. They arrived multicast cell is hold on in an exceedingly memory pool and is joined by its address tokens. supported the planning selections from the planning algorithms dead on the address tokens, the multicast cell is distributed and is off from the memory till all its destinations ar reached. The FIFOMS and CMF are ready to attain low latency and high outturn, however the bottlenecks of the design will hinder its measurability. However, the hardware complexness of the address token generator are often O(N), since up to N tokens ar generated for every inward cell, and also the address token generating rate is needed to be N times the cell arrival rate thanks to that multiple tokens ar generated for every inward cell at intervals one cell TRM. Besides, this design needs a posh buffer management mechanism to send a multicast cell victimization the link address in associate address token as a result of the particular cell to be sent isn't invariably the HOL cell. Nick McKeown, and Ritesh proposed an increasing proportion of traffic on the web is multicast, with users distributing a large kind of audio and video material. it's assumed that: 1) every input maintains one queue for inward multicast cells and 2) solely the cell at the pinnacle of line are often determined and regular at only once. The hardware is needed to be: 1) work protective, which implies that no output port could also be idle as long as there's Associate in nursing input cell destined to that and 2) honest, which implies that no input cell could also be command at HOL for over a set variety of cell times. The aim of our work is to search out a work-conserving, honest policy that delivers most turnouts and minimizes input queue latency, and however is easy to implement in hardware. once a programming policy decides that cells to schedule, competition might need that it leave a residue of cells to be regular within the next cell time. the choice of wherever to put the residue unambiguously defines the programming policy. Subject to a fairness constraint, we tend to argue that a policy that continuously concentrates the residue on as few inputs as attainable typically outperforms all different policies. We discover that there's a trade-off among concentration of residue, strictness of fairness, and implementation simplicity. By mapping the final multicast shift drawback onto a variation of the popular block-packing game Tetris, we tend to are ready to analyze, in Associate in nursing intuitive and geometric fashion, varied programming policies that possess these attributes in numerous proportions. we tend to gift a unique programming policy, known as TATRA, that performs very well and is strict in fairness. we tend to conjointly gift an easy weight-based formula, called WBA, that is\ easy to implement in hardware, fair, and performs well in comparison to a concentrating formula. One such approximation, TATRA, is motivated by Tetris, the popular block-packing game. TATRA avoids starvation by employing a strict definition of fairness, whereas scrutiny well to the performance of Concentrate. The second formula, WBA, is intended to be terribly easy to implement in hardware, and permits the designer to balance the trade-off between fairness and turnout. Zhiyang Guo and Yuanyuan Yan propose a novel optical buffer known as multicast-enabled Fiber-Delay-Lines which may offer versatile delay for copies of multicast packets victimization solely a little variety of FDL segments. we tend to then gift a Delay-Guaranteed Multicast programming algorithmic rule that considers the schedule of every inbound packet for multiple time slots. we tend to conjointly discuss some fascinating options of DGMS intimately, like bonded delay bound and adaptively to transmission needs. To relax the time constraint of DGMS, we tend to additional propose a pipelining technique that distributes the programming tasks among a sequence of sub-schedulers. The combinatorial logic circuit style of every sub-scheduler, that additional reduces time quality, is additionally provided. The performance of DGMS is tested extensively against applied mathematics traffic models and real net traffic, and therefore the results show that the planned DGMS algorithmic rule can do ultra-low average packet delay with minimum packet drop quantitative relation. Multicast programming in optical packet switches with FDLs buffer is considerably totally different from the well-studied multicast programming in electronic switches for the explanation that each one the approaches for electronic switches trust electronic RAM to resolve output competition, whereas FDLs will just delay packets for a set period of your time. many multicast programming schemes victimisation FDLs as buffer are planned. Among them, a wide adopted theme is output buffering during which associate degree output buffer consisting of associate degree N ×B switch and B FDL segments with fastened progressive delay is placed at every output. Throughout every programming cycle, the hardware assigns a FDL phase with correct delay in every output buffer to the packets destined for that output. to attain an affordable packet ratio and network link utilization, the output buffering theme needs an oversized quantity of FDL segments to construct output buffers. Since FDLs area unit large, such associate degree approach isn't ascendible for giant switches.

3. Switch Architecture and Buffer Management

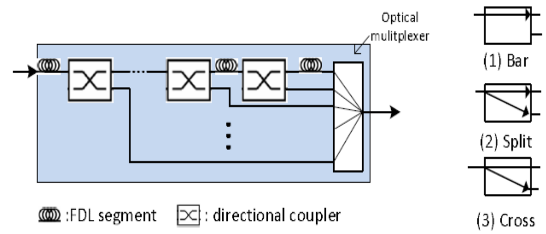

Fig: 2. Multicast-enabled FDLS (M-FDLs). Left: The structure of M-FDLs. Right: Three possible states of the directional coupler: bar, split and cross.

In this section, we tend to shortly describe the adopted switch architecture and also the operation of the projected optical buffer called multicast-enabled FDLs (M-FDLS). We tend to take into account an easy single-wavelength, input-buffered optical multicast packet switch, the high level read of that is shown in Fig. 1. The adopted switch consists of optical multicast switch cloth And M-FDLs as input buffers within the data-plane, and optical label processors and electronic hardware within the management plane. We assume the switch operates during a time-slotted manner and all optical packets have identical length. every optical packet consists of 2 parts: payload and label (or header). The optical label contains the destination outputs of the packet, and is far shorter than the optical payload. once associate optical packet arrives at associate input, its label is stripped off and sent to the label processor, which may be performed passively by the optical correlation technique. The label processor then converts all optical headers to the electronic kind, and sends them to the electronic hardware, that calculates the schedule for every packet. Note that the optical label will adopt a lower bit rate than the optical payload to facilitate electronic planning [14]. Based on planning results, management signals square measure issued to the FDL buffers and switch cloth to properly put together the switch. Next, we tend to gift a unique optical buffer referred to as multicast enable FDLs (M-FDLs) that has versatile delay for every incoming multicast packet. Fig. a pair of shows the buffer structure. The M-FDLs buffer consists of cascaded couplers and FDL segments, and every phase will offer a delay of T, the duration of a time interval. to produce versatile delays locomote from T to dT , a complete of d FDL segments square measure required. For each coupler, there square measure 3 states: once it's in “bar” state (the default state), packets merely bear it and move to the next FDL segment; once the state is “split,” a replica of packet will be sent to the switch for transmission although associate optical multiplexer, whereas the packet continues to maneuver forward in the M-FDLs; once the state is “cross,” packets can move out of the M-FDLs utterly and be sent to the switch for transmission. The compensation for the ability loss and noise incurred from optical rending aren't shown within the figure. Let’s use associate example maybe however the M-FDLs operates. Assume that a multicast packet arrives at time interval t, and is scheduled to deliver a replica of it to a number of its destination outputs within the (t+i)th time interval and to the remainder of its destination outputs within the (t+j)th time interval (i <

At the start of the (t+i)th time interval, the packet moves to the ith coupling, and the hardware sets the ith coupling to "split," specified a copy of the packet are sent to the switch materials. At the beginning of the (t+j)th time interval, the hardware sets the jth coupling to "cross" state, so the packet moves out of the M-FDLS and be transmitted utterly. Compared with existing FDL a buffer for multicast packet switching, M-FDLs has some clear blessings. On one hand, M-FDLs doesn't have the matter of restricted multicast processing capability within the recirculating loop buffer within the wavelength-assisted routing theme [4], [13], since it are often shared by all the incoming multicast packets during a pipelined fashion. On the opposite hand, M-FDLs uses abundant less FDL segments compared to the output buffer employed in the output buffering theme [12]. for instance, to attain versatile delays ranging from 1T to 16T , every output buffer in [12] needs (1+2+· · ·+16 = 138) FDL segments, whereas every M-FDLs only needs sixteen FDL segments, that could be a substantial saving. Based on the input-buffered optical multicast packet switch and M-FDLs buffer delineated higher than guaranteed multicast programming

4. Guaranteed Multicast Scheduling

One fascinating feature of GMS is that the utmost packet delay for any transmitted packets is finite by D, wherever D is that the variety of programing vectors, in spite of traffic conditions. If output copies of some packets can't be scheduled for subsequent D time slots, the computer hardware will promptly drop them. As are seen within the performance analysis section, packet drop solely happens once network is extremely engorged and may be unbroken at a minimum level with an inexpensive variety of programming vectors D. additionally, DGMS is extremely adaptation to traffic conditions, that means that the trade-off between the packet drop magnitude relation and therefore the average delay may be simply adjusted by dynamic the quantity of programming vectors D. If traffic is delay-sensitive, a smaller D will filtrate packets with long delay and win ultra-low latency, whereas a bigger D makes the computer hardware additional tolerant to packet delay and at risk of reliable packet transmission. GMS also can give fairness guarantee, since every inbound packet is assigned per its input index during a spherical robin fashion. Finally, the quantity of FDL segments GMS needs is way smaller compared to existing multicast programming algorithms for Roman deity. The time complexness of GMS is O (N2D) within the worst case, wherever N is that the switch size and D is that the variety of programming vectors. Next we are going to introduce a pipelining technique to additional scale back the complexness to O (N).

A. Scheduling Method

DGMS permits the packets arrived later to be transmitted before the packets arrived earlier, therefore eliminates the Head-of-Line (HOL) interference. for instance, packet (1)from input three (blue block) arrived just one occasion slot later than packet (2, 4) (grey block), however is scheduled to be transmitted earlier. Such a feature permits additional economical buffer management and reduces packet delay. However, it's price mentioning that so as transmission of packets from identical flow (i.e., packets sharing identical input and fan-out) is warranted in DGMS, because it is not possible to deliver a later packet before its forerunner within the same flow in DGMS.

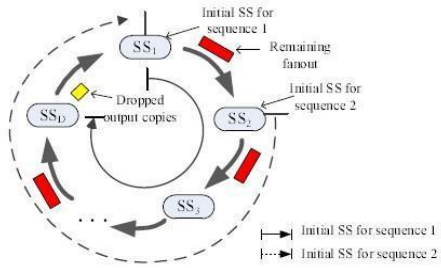

Fig: 3. Scheduling Method

In GMS, all the programming vectors and mask vectors got to be shifted forward by one position at the start of every slot that involves huge knowledge transfer among the vectors. To simplifies the operation, we tend to clear the initial SS then "rotate" right-handed by one position at the start of each slot, that is, opt for the one next to the initial SS because the initial SS within the next slot. within the next slot, SS2 is chosen because the initial SS. during this manner, SS1 becomes the last SS within the sequence and every one alternative SS's square measure one position nearer to the initial SS, indicated by the dotted line. the easy rotation avoids huge knowledge transfer and solely takes O (1) time, whereas manufacturing equivalent results thereto of shifting all the vectors forward.

5. Result and Discussion

A. Experimental Results

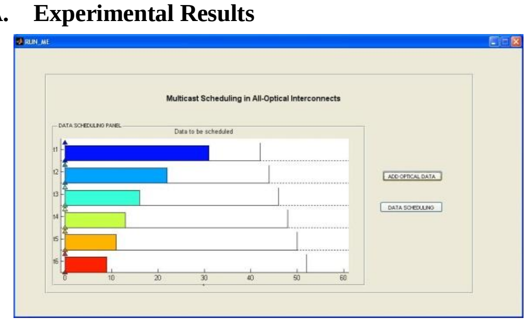

Fig: 4. Adding data in to Optical Interconnects

The data and its due time can be added in the system up to user defined level. Depending on the data length and duration time the chart can be plotted.

B. GMS scheduling with Single out port

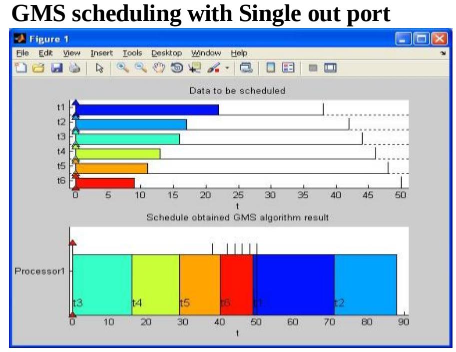

Fig: 5. GMS scheduling with single out port

Arrived data can be scheduled using GMS algorithm .depending on the time slot provided by the user the data can be arrived in the output port. Interconnect has single output port each data will be arrived in output port with different time slot.sue to time slot split in the circuit drop ratio must be reduced

C. GMS scheduling with Multiple out port

Arrived data can be scheduled using GMS algorithm .depending on the time slot provided by the user the data can be arrived in the output port. Interconnect has multiple output port each data will be arrived in output port with different time slot. More output port leads to time slot split in the circuit drop ratio must be reduced

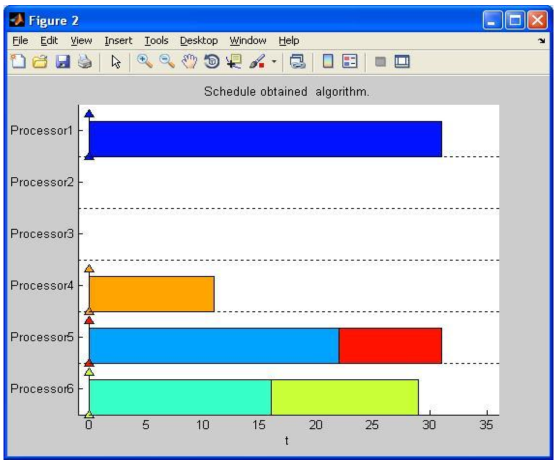

Fig: 6. GMS scheduling with multiple out port

D. Drop ratio comparison for GMS VS LLMS

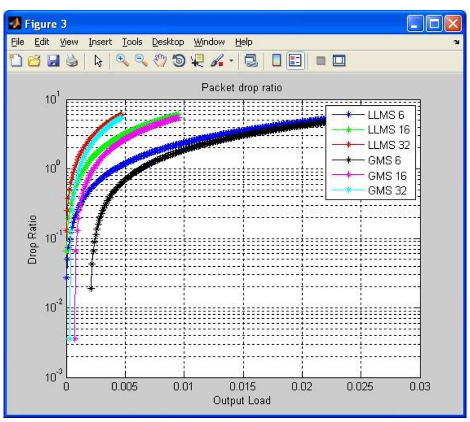

Fig: 7. Drop ratio comparison for GMS VS LLMS

The average drop ratio of LLMS and GMS under various interconnects are shown in Fig. The packet drop ratio of LLMS is slightly higher than that of GMS, which indicates that GMS can achieve near optimal packet drop ratio. Compares the average packet latency of LLMS and GMS it can be seen that, as the traffic load increases performance of interconnects can be high in GMS algorithm. GMS theory that can maintain sustainability under all admissible multicast traffic conditions. We also observe that GMS 16 performs better than GMS 32 in terms of average packet latency. The reason is that with more scheduling vectors, the scheduler is less prone to drop packets and more tolerant to packet latency.

6. Conclusion

In this paper, we've studied multicast programming downside for input-buffered optical multicast switches. we tend to 1st planned an economical optical buffer referred to as multicast-enabled FDLs (M- FDLs), which may give versatile delay for output copies of each multicast packet whereas requiring solely atiny low variety of FDL segments. we tend to conjointly designed a delay-guaranteed multicast scheduling (DGMS) rule, the most options of which may be summarized as follows.

- Bonded delay boundary for transmitted packets. DGMS will guarantee a set delay boundary for all transmitted packets, whereas keeping packet drop quantitative relation ata minimum level even below the foremost full traffic condition.
- Ultra-low average delay. DGMS will observe and promptly drop output copies with long delay, so will considerably lower the typical delay.
- Adaptational to varied transmission necessities. DGMS can simply regulate the quantity of programming vectors D to balance the trade-off between the packet drop quantitative relation and the packet delay.
- Need only a few variety of FDLs. compared to exist-ing multicast programming schemes for all optical packet switches, DGMS are able to do superior performance exploitationmuch less FDLs.
- Fairness. All packet arrivals area unit regular in an exceedingly spherical robin fashion to confirm fairness. We conjointly given a pipelining technique and combinatorial digital circuit style for DGMS, that lowers the time complexity to O(N). in depth simulations demonstrate that DGMS achieves ultra-low average packet delay below each statistical traffic models and real web traffic with a least packet drop quantitative relation.

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