FPGA Design of Low Power Launch-Off-Shift and Launch-Off-Capture Testing

R. Veeramani *, S. Devi Poonguzhali
Department of Electronics and Communication Engineering, K. Ramakrishna College of Technology, Samayapuram, Trichy, Tamil Nadu, India

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Abstract
At-speed or even faster-than-at-speed testing of VLSI circuits aims for high-quality screening of the circuits by targeting performance-related faults. On one hand, a compact test set with highly effective patterns, each detecting multiple delay faults, is desirable for lower test costs. On the other hand, such patterns increase switching activity during launch and capture operations. Patterns optimized for quality and cost may thus end up violating peak-power constraints, resulting in yield loss, while pattern generation under low switching activity constraints may lead to loss in test quality and/or pattern count inflation. In this paper, we propose design for testability (DfT) support for enabling the use of a set of patterns optimized for cost and quality as is, yet in a low power manner; we develop three different DfT mechanisms, one for launch-off shift, one for launch-off capture, and one for mixed at-speed testing. We propose the efficient BISR (Built in self repair) designs based on fail-pattern identification. We also propose binary matrix lossless compression algorithm to compress the test patterns in test cubes.

1. Introduction

AT-SPEED or even faster-than-at-speed testing of VLSI circuits aims for a high-quality screening of VLSI circuits by targeting performance-related faults. Scan-based at speed testing necessitates load, launch, and capture operations for every test pattern. Load operation is performed via scan/shift operations, filling up all the scan chains with the pattern. As the targeted defects are timing-related, these patterns need to check whether transitions launched from scan cells can arrive at their destinations (scan cells) within a functional clock period. There are mainly two different schemes for launching transitions off the serially loaded pattern. In the launch-off capture (LOC or broadside) test [3], a functional capture operation launches transitions from the locations where the serially loaded pattern (V1) differs from the response of the combinational logic to V1, i.e., the launch pattern (V2). In launch-off-shift (LOS or skewed-load) test [4], a single cycle shift operation launches transitions from the locations where the serially loaded pattern (V1) differs from its one-bit shifted version, i.e., the launch pattern (V2). In both schemes, a subsequent fast functional capture operation, which is of a functional clock period apart from the launch event, sets a deadline for the transitions to arrive at their destinations; a timing-related defect that slows down the chip below its rated clock speed is thus exposed. Yield loss problems are experienced in at-speed testing schemes [5]–[8]. Excessive switching activity during the launch cycle may result in elevated peak supply currents, leading to IR drop that increases the signal propagation delays in the combinational logic. The end effect cannot be differentiated from that of a timing-related defect, causing a functional chip to fail the at-speed test. Peak power during the launch cycle of at-speed testing should therefore be reduced in order to avoid the yield loss induced by IR drop. Significant research efforts have been expended in reducing power dissipation during the launch and capture of at speed testing.

Corresponding Author,
E-mail address: veerahasan.mani@gmail.com

2. Literature Survey

Test pattern generation while accounting for the functional clock gating logic in order to produce patterns that disable parts of the design during launch and capture has been proposed in [9] and [10] to reduce peak power at the expense of pattern count inflation. Another approach that elevates pattern count while reducing peak launch power has been in the form of generating patterns under the constraint that only one chain launches transitions while all chains capture them [11]. Another similar scan-segmented solution [12] partitions the scan cells into three regions where only two out of three regions launch and capture any test pattern. A partitioning approach has been proposed in [13] where power wise costly patterns are further analyzed via fault simulation to identify the location of the care bits, which dictate the partitioning of the design during capture; with few problematic patterns, such an approach can deliver power savings. X-fill approaches have also been proposed [14], [15] where pattern count inflation is the side effect. Partitioning the design and testing one partition at a time has been proposed to reduce launch and capture power in built-in self-test (BIST) [16], in LOS [17] and in LOC [18] testing schemes; in all these schemes, newly generated patterns targeting one partition at a time end up loading the interface registers of other partitions as well, incurring test time and data volume penalty. Similarly, pattern count increase has been experienced even when the design is partitioned via ILP that minimizes capture violations [19]; additional test patterns, possibly of a high sequential depth, need to be generated for the faults missed due to capture violations. Finally, low-power automatic test pattern generation (ATPG) solutions have also been proposed [20]–[23]. In this paper, we propose a test power reduction framework for LOS-based and LOC-based at-speed testing.

The contribution of this paper is a design partitioning technique that can reduce power dissipation during launch and capture operations in at-speed testing. Our goal is to reuse the patterns generated (and optimized for pattern count and quality) by a conventional power-unaware transition/path-delay ATPG tool intact, and yet apply them in a low power manner, a feature that other partitioning solutions fail to deliver; this way, not only pattern count and test quality (fault and ancillary defect coverage) are retained intact, but also the test generation process is neither modified nor repeated. This comes at the cost of added design for testability (DfT) circuitry. For tight area budgets, the trade-off version of the proposed techniques should be utilized in order to control the area cost while reducing peak launch/capture power

3. Existing Method

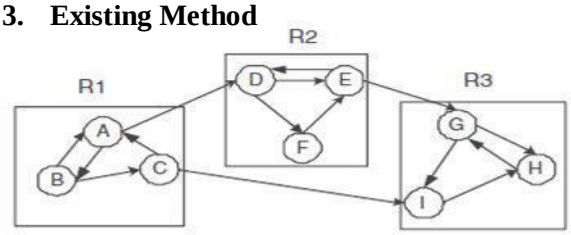

Fig: 1. LOC Testing one region at a Time

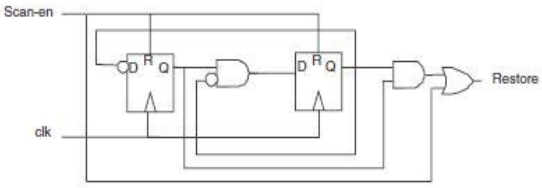

Fig: 2. Restore Operation

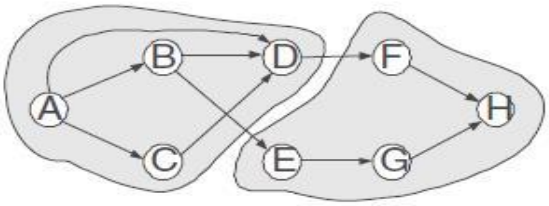

Fig: 3. LOS Test one Region at a Time

We illustrate the proposed low-power LOS testing strategy in Fig. 2, where the eight SCCs shown are partitioned into two regions (A, B,C, D) and (E, F, G, H) during launch and capture operations. This time, a rewind signal is used to make the interface registers shift in the reverse direction for a single cycle, restoring their load state. In the proposed algorithm, we iteratively merge SCCs into larger regions. The end result of each merge operation is potentially the elimination of some of the interface registers, and thus saving area cost, and potentially an increase in launch or capture power. In every step, the two regions, whose merge eliminates a maximum number of interface registers, are merged; every step reduces the number of regions by 1, as a result.

4. Proposed Method

4.1 Binary Matrix Lossless Compression Method

The binary matrix lossless compression method is done via the construction of binary matrix and grayscale matrix. Below the conditions are used to calculate the binary matrix and grayscale matrix. and also decompressed condition was described. So the compression algorithm used to lead the power reduction in the testing.

$$[BM]_{i,j} = \begin{bmatrix} 0 & \text{if} \quad [OR]_{i,j} = [OR]_{i,j+1} \\ 1 & \text{otherwise} \end{bmatrix}$$

$$[GSM]_k = \begin{bmatrix} \text{nul} & \text{if} \quad [OR]_{i,j} = [OR]_{i,j+1} \\ [OR]_{i,j} & \text{otherwise} \end{bmatrix}$$

$$[rec\_img]_{i,j} = \begin{bmatrix} [GSM]_k & \text{if} \quad [BM]_{i,j} = 0 \\ [GSM]_{k+1} & \text{if} \quad [BM]_{i,j} = 1 \end{bmatrix}$$

4.2 BISD (Built In Self Repair)

The efficient built in self repair method was used to find the error sequence in the test patterns. Below the procedures are followed for find the error patterns. And this method also lead to the power reduction in testing.

- **Step1**:
  Find syndrome pattern of the test vectors as follows:
  Syndrome1=rx[2]^rx[3]^rx[4]^rx[7];
  Syndrome2=rx[1]^rx[2]^rx[3]^rx[6];
  Syndrome3=rx[3]^rx[4]^rx[1]^rx[5];
- **Step 2**:
  If syndrome is 011 then the bit rx[2] is corrupted.
  If syndrome is 101 then the bit rx [4] is corrupted.
  If syndrome is 110 then the bit rx[1] is corrupted.
  If syndrome is 111 then the bit rx[3] is corrupted.
- **Step3:**
  Find the er bit=rx[1]^rx[2]….^rx[7].
- **Step4:**
  If the er==1,then error=1 else error=0;
- **Step5:**
  If error==1,then the test pattern is corrected as follows: New pattern=old_pattern+rx;

5. Simulation Results

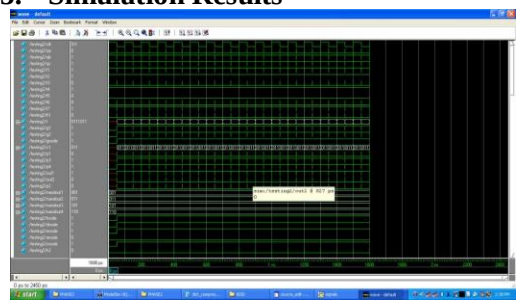

Fig: 4. Wave form Result of Testing

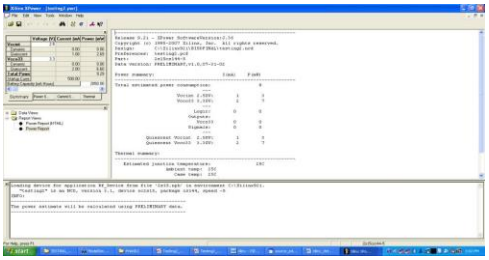

Fig: 5. Power report

6. Conclusion

We planned DfT maintain that can restore the load state in interface registers in between the launch/capture operations in the design regions, enabling low-power LOC,LOS, and mixed at-speed testing. This way, a set of patterns optimized for cost and quality can be utilize as is, yet in a small power manner.

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