DESIGN OF SQRT CSLA FOR LOW POWER MULTIPLIER

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***Abstract*—In this paper, we propose a reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT)architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified**.

Keywords—ANT , RPR, low power

I. INTRODUCTION

THE RAPID growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To lower the power dissipation, supply voltage scaling is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage [1]. However, in deep-sub micrometer process technologies, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, the design techniques to enhance noise tolerance have been widely developed [2]–[12]. An aggressive low-power technique, referred to as voltage over scaling (VOS), was proposed in [4] to lower supply voltage beyond critical supply voltage without sacrificing the throughput. However, VOS leads to severe degradation in signal-to-noise ratio (SNR). A novel algorithmic noise tolerant (ANT) technique [2] combined VOS main block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant energy saving. Some ANT deformation designs are presented in [5]–[9] and the ANT design concept is further extended to system level in [10]. However, the RPR designs in the ANT designs of [5]–[7] are designed in a customized manner, which are not easily adopted and repeated.

The RPR designs in the AN designs of [8] and [9] can operate in a very fast manner, but their hardware complexity is too complex. As a result ,the RPR design in the ANT design of [2] is still the most popular design because of its simplicity. However, adopting with RPR in [2] should still pay extra area overhead and power consumption. In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block in [2]. Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead.

We take use of probability, statistics, and partial product weight analysis to find the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

II. ANT ARCHITECTURE DESIGNS

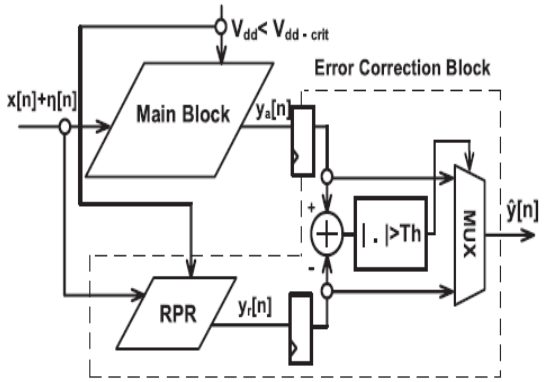

Fig.1.Ant Architecture

The ANT technique [2] includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay *T*cp of the system becomes greater than the sampling period *T*samp, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique [2], a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output *ya*[*n*]; however, RPR output *yr* [*n*] is still correct since the critical path delay of the replica is smaller than *T*samp [4]. Therefore, *yr* [*n*] is applied to detect errors in the MDSP output *ya*[*n*]. Error detection is accomplished by comparing the difference |*ya*[*n*] − *yr* [*n*]| against a threshold *Th*.

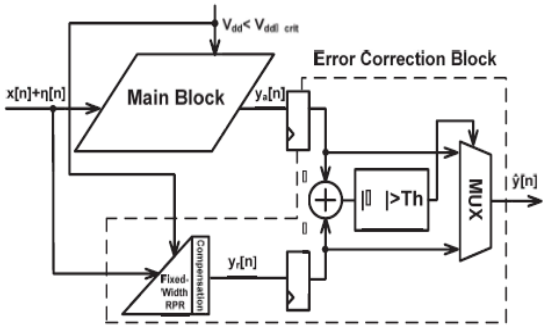

Fig.2. External Architecture of Fixed Width RPR

Threshold voltage can be calculated by using this equation,

$$\hat{y}[n] = \begin{cases} y_a[n], & \text{if } |y_a[n] - y_r[n]| \le Th \\ y_r[n], & \text{if } |y_a[n] - y_r[n]| > Th. \end{cases}$$

$$Th = \max_{\forall input} |y_o[n] - y_r[n]|$$

Once the critical path delay Tcp of the system becomes greater than the sampling period Tsamp, the soft errors will occur. It leads to severe degradation in signal precision. The output response from RPR circuit yr(n) is used to detect the errors in the output response of the main block.Error detection is accomplished by comparing the difference |ya[n] − yr [n]| against a threshold Th.Once the difference between ya[n] and yr [n] is larger than Th, the output ˆy[n] is yr [n] instead of ya[n].

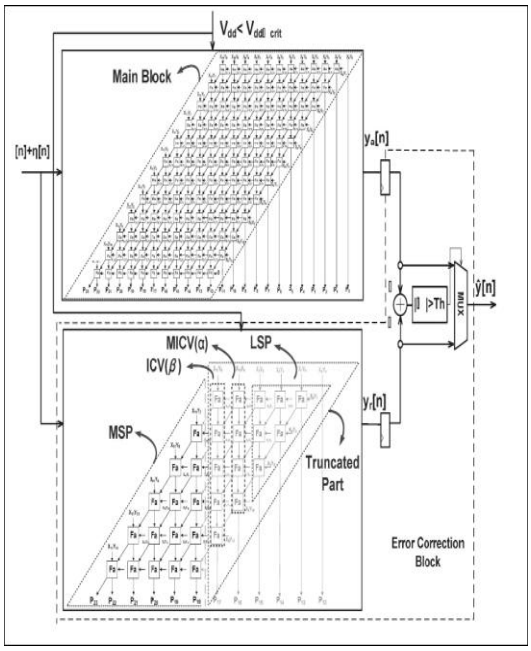

Fig.3. Internal Architecture of Fixed Width RPR

II.SIMULATION RESULTS

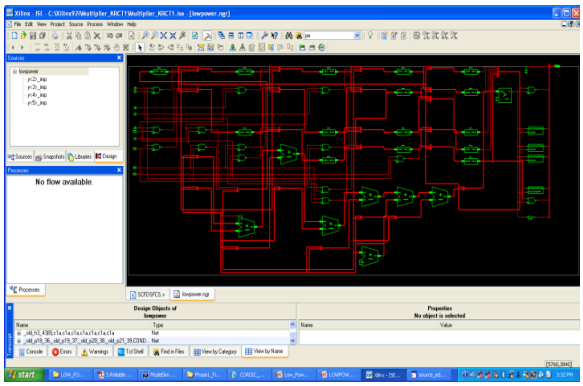

Fig.4.Schematic view of RPR.

Below figure shows the simulation waveform of Fixed width RPR.

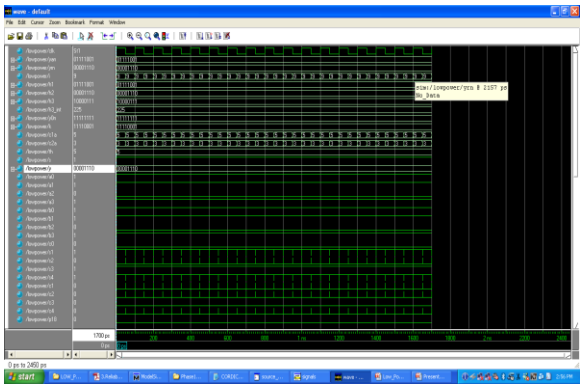

Fig.5.simulation waveform of RPR

Below table shows the performance comparison of Fixed width RPR and Full width RPR.

Performance Comparison:

Methodology	Power Consumption
Proposed	0.038mW
Conventional	0.393mW

Table.1.comparision of PowerConsumption

V. CONCLUSION

In this paper, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC90-nm process and its silicon area is 4616.5 μm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mW. In the presented 12-bit by 12-bitANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltagein our ANT design can be lowered to 0.623 VDD, and powerconsumption in our ANT design can be saved by 23% ascompared with the state-of-art ANT design.

V.REFERENCES

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