Energy-efficient error control approach for on chip interconnects using Hamming product codes

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ABSTRACT

To achieve high To speed, energy efficient and reliable on-chip communication, solutions that can simultaneously address multiple logic errors and crosstalk-induced delay uncertainty are needed. In this dissertation, we propose a method for combining Hamming product codes and type-II hybrid automatic repeat request (HARQ) with skewed transitions to address this critical issue.As technology scales, interconnects are becoming susceptible to multiple random and burst errors, requiring more powerful error control coding (ECC) techniques than those previously used. We propose the combination of Hamming product codes with type-II HARQ to provide a strong yet energy-efficient error control approach for on chip interconnects. We analyze the performance of the proposed method in terms of the required number of wires, codec delay and residual flit error rate. Two design scenarios are investigated. For implementation with low link swing voltages, the combination of Hamming product codes with type-II HARQ are shown to meet the same reliability requirements as previous solutions while using a lower link swing voltage, reducing energy consumption. The proposed method can also be integrated into a configurable error control approach by combining it with a traditional Hamming code. The different coding strengths provided by this realization can achieve better energy performance in the presence of varying noise conditions.

I. Introduction

As technology scales into the nano scale regime, reliability is becoming a major challenge for on-chip interconnects. Interconnect reliability issues are caused by manufacturing defects or a variety of noise sources, such as external radiation crosstalk coupling supply voltage fluctuations. process variations temperature variations electromagnetic interference (EMI) and combinations of these sources. Manufacturing defects can cause open connections or shorted connections in on-chip interconnect (e.g.,over etching or cracks caused by material stresses) eventually leading to logic errors.

Noise sources affect the reliability of on-chip interconnect in two way signal integrity and delay uncertainty. Noise sources reduce the signal integrity of on-chip interconnect by inducing voltage glitches. If a voltage glitch is greater than the tolerable noise margin of the circuit and has asufficient duration, it can causelogic errors. Delay uncertainty refers to an unknown fluctuation in the timing of a Signal transition. Delay uncertainty decreases the system operating frequency because a large design margin is required to guarantee correct operation. In nanoscale technology, crosstalk-induced delay uncertainty can be a critical bottleneck for the operation of high speed synchronous systems.

Crosstalk coupling is one of the most important factors affecting reliability of on chip interconnects. Crosstalk coupling is caused by the mutual capacitance or mutual inductance between wires. consisting of the parallel plate capacitance *Cg1* between substrate or ground and the parallel surface of a wire, fringing capacitance *Cg2* between a substrate or ground and the sides of a wire, and the coupling capacitance *Cc* between two adjacent wires. As technology scales, the interconnect thickness *Tint* scales at a slower rate than the interconnect width *Wint* and spacing *Sint*. Thus, the interconnect aspect ratio, defined as the ratio of *Tint* to *Wint*, increases with each technology node. The increased interconnect aspect ratio has caused an increase in capacitive coupling effects.

Inductive coupling occurs when signal switching causes a change in Magnetic field. The gigahertz clock frequencies in nanoscale technology result in a

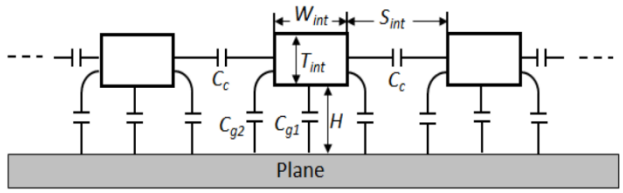

Figure 1.Parallel Plate, Fringing And Coupling Interconnect Capacitances

non-negligible inductive effect in on-chip interconnects. Unlike capacitivecoupling, inductive coupling can be a long range phenomenon and is more important in the presence of wide busses.

II.Literature review

To achieve high speed, energy efficient and reliable on-chip communication, solutions that can simultaneously address multiple logic errors and crosstalk-induced delay uncertainty are needed. In this dissertation, we propose a method for combining Hamming product codes and type-II hybrid automatic repeat request (HARQ) with skewed transitions to address this critical issue. As technology scales, interconnects are becoming susceptible to multiple random and burst errors, requiring more powerful error control coding (ECC) techniques than those previously used. We propose the combination of Hamming product codes with type-II HARQ to provide a strong yet energy-efficient error control approach for onchip interconnects. We analyze the performance of the proposed method in terms of the required number of wires, codec delay and residual flit error rate. The proposed method is shown to achieve several orders of

magnitude reduction in residual flit error rate compared to previous solutions when multiple random and burst errors are considered. Two design scenarios are investigated. For implementation with low link swing voltages, the combination of Hamming product codes with type-II HARQ are shown to meet the same reliability requirements as previous solutions while using a lower link swing voltage, reducing energy consumption. The proposed method can also be v integrated into a configurable error control approach by combining it with a traditional Hamming code. The different coding strengths provided by this realization can achieve better energy performance in the presence of varying noise conditions. Further, the inherent skew resulting from the ECC parity generation is exploited to ensure that no two adjacent wires switch in opposite directions simultaneously, thereby reducing worst-case on-chip capacitive coupling. Instead of waiting for the parity computation to send the original input data and parity bits to the link at the same time, we send the original input data before the parity bits are available. A mapping algorithm is proposed to properly map data and parity check bits to link driver registers, which are triggered by alternating clock phases. The proposed method hides the delay insertion overhead of conventional skewed transition methods. Compared to other solutions that simultaneously handle logic errors and delay uncertainty, the proposed method requires fewer wires, resulting in smaller link area and energy consumption.

III. EXISTING SYSTEM

Common approach of arbitrarily combining different coding schemes lead to high complexity design. The proposed approach exploits the inherent characteristics of joint wire duplication and error control policies, and systematic codec integration for reduced hardware complexity in providing adaptable error protection levels while maintaining $(1+2\lambda)\tau 0$ CIBD. The proposed scheme works in three modes; i.e. normal mode and two power saving modes namely duplicated SECDED (D_SECDED), shielded SECDED (S_SECDED), and shielded SEC (S_SEC) respectively. Normal or D_SECDED mode provides highest error protection at no power saving while the two power saving modes (S_SEC, S_SECDED) provide moderate and low error protection leading to moderate and high power saving respectively. In D_SECDED mode, JTEC-SQED scheme is selected which uses duplication and HARQ-based Hamming SECDED as the crosstalk avoidance and error control respectively. JTEC-SQED is employed as it achieves high error protection; i.e. triple error correction, quadruple error detection and willbe used in high noise condition. The drawback of this scheme is the increased bus power consumption due to the switching of the duplicated wires and complex decoding algorithm. In the power saving modes, the crosstalk avoidance approach is switched to shielding technique while the error control schemes used are HARQ-based Hamming SECDED and FEC-based Hamming SEC for S_SECDED and S_SEC modes respectively. S_SECDED mode enjoys error protection up totwo error detection while S_SEC has single error correction, thus will be used in moderate and low noise conditions respectively.

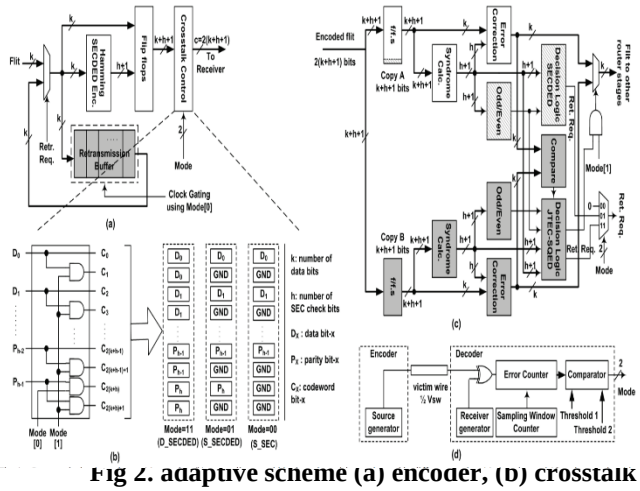

Fig 2. adaptive scheme (a) encoder, (b) crosstalk control block and resulting codeword in different modes, (c) decoder, and (d) noise monitor block.

IV.PROPOSED SYSTEM

Error control coding (ECC) has been successfully applied to improve the reliability of on-chip interconnect by correcting logic errors. Unfortunately, ECC is inefficient to address crosstalk-induced delay uncertainty, which greatly decreases the system performance and can also cause timing errors. Crosstalk-induced delay uncertainty results from the dependence of coupling capacitance and inductance on different wire switching patterns. In this dissertation, we mainlyfocus on thereduction in capacitive coupling effects. Crosstalk-induced delay uncertainty can be alleviated by techniques such as shielding, routing, wire sizing and spacing, crosstalk avoidance codes (CAC), skewed transitions, and staggered repeater. Typically, these methods do not address logic errors. To achieve reliable on-chip communication, solutions that can simultaneously address logic errors and crosstalk-induced delay variations are needed.

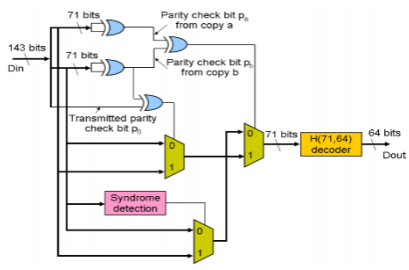

Figure. 3 The implementation of CADEC decoder

The input data is assumed as 64-bit. For Hamming product code, *k2*=4 is used to minimize the number of wires in the link. Because the number of rows is even in the Hamming product code, an extra wire is inserted to ensure

the correction of the mapping algorithm. The results show that the proposed method requires fewer wires to simultaneously address multiple logic errors and crosstalk-induced delay variations. The proposed method also achieves a better decoder delay. The codec area of the proposed method increases; while codec area is much smaller compared to the global link area. The results show that the use of product codes achieves a much lower residual flit error rate compared to CADEC code, because the decoding algorithm in can only correct double errors; while the proposed method can effectively correct multiple random and burst errors.The proposed crosstalk reduction method can achieve superior reliability and energy consumption.

V. IMPLEMENTATION

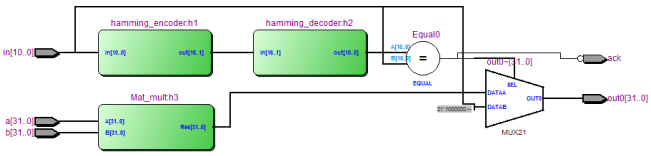

Figure 4 Cross Talk Aware Multiple Error Control

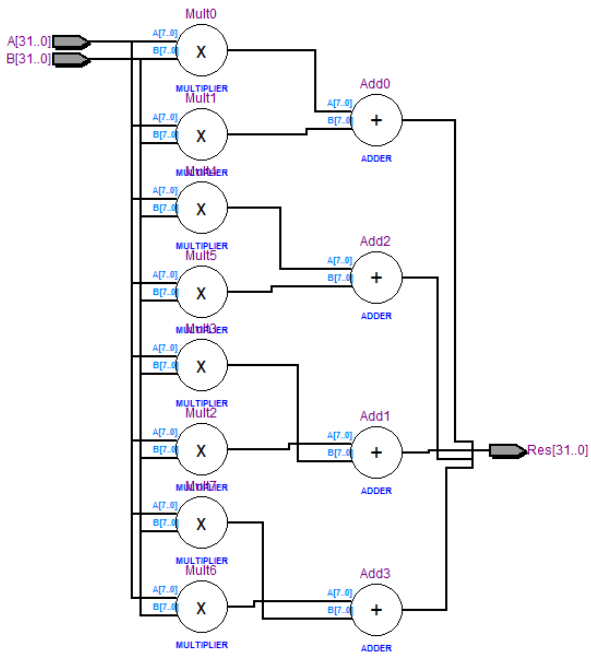

Figure 5 Matrix Block In RTL View

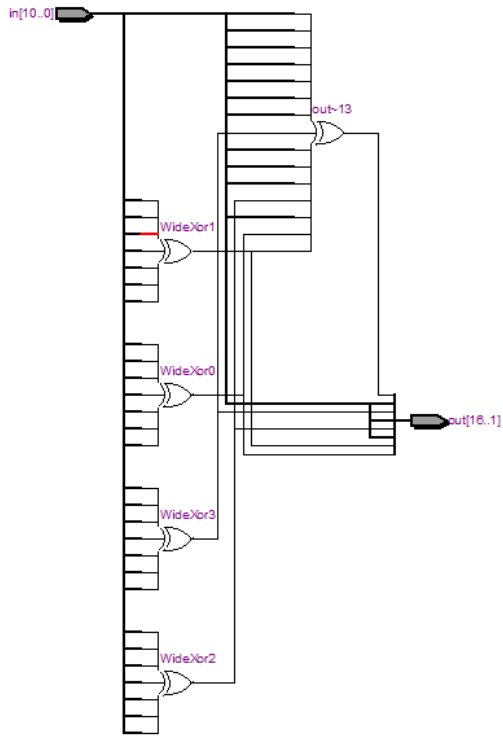

Figure 6 Hamming Encoder

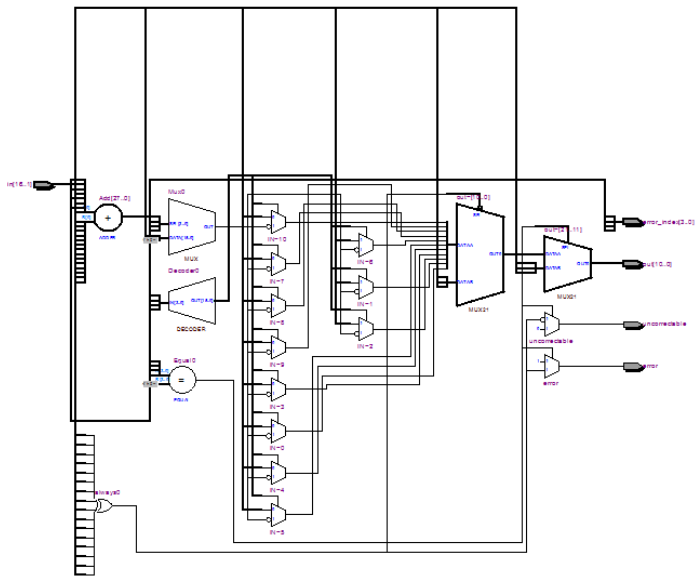

Figure 7 Hamming Decoder

VI. RESULT

Table 1 Power Calculation

Total Thermal Power dissipation	122.9mW
I/O Power dissipation	79.97mW
Core Static thermal power Dissipation	42.82mW

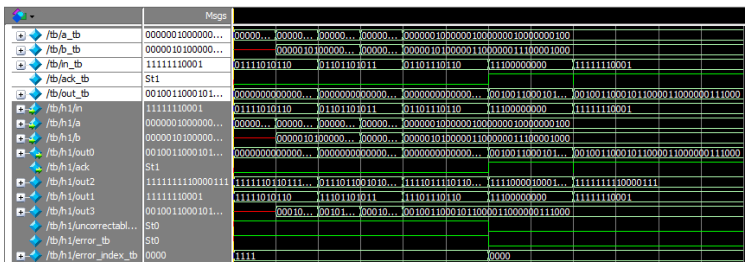

Figure 8 Waveform Output

VII.Conclusion

This dissertation presents a solution to simultaneously address multiple logic errors and crosstalk-induced delay uncertainty. Multiple errors are becoming a critical issue for on-chip interconnect in nanoscale technology, requiring more powerful error control schemes to maintain reliable on-chip communication. At the same time, interconnect energy consumption is becoming an increasingly large portion of on chip power dissipation, motivating the need for more energy efficient communication solutions. In this dissertation, we propose an error control scheme combining Hamming product codes with type-II HARQ to balance reliability and energy efficiency. The proposed method can efficiently handle multiple random and burst errors while greatly reducing the overhead (in terms of number of wires and energy consumption) compared to a direct product code implementation. To further improve the reliability of on-chip communications, we propose a new solution to incorporate crosstalk reduction into the error control coding. This method provides large improvements over other techniques combining both error control coding and crosstalk avoidance.

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