HIGH SPEED WEIGHTED BASED NOC ARCHITECTURE WITH ROUTER FAULT DETECTION

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ABSTRACT

To manage ever increasing complexity, advanced System- on-Chip (SoC) designs typically encompass a system integration process based on existing computation, storage and interconnect IPs .These IPs are designed separately, following a common interface, AMBA, AXI, OCP-IP etc. Later, the computation and storage IPs are integrated together with the interconnect IP. While a common interface smoothes the hardware integration, guaranteeing application performance during the integration remains an open challenge because of traffic diversity and unpredictability. This is becoming a critical issue as advanced SoC interconnects are moving from bus to network-on-chip (NoC) architectures in order to accommodate hundreds of IPs, which raise complexity and performance uncertainty in orders of magnitude.Flow regulation is a traffic shaping technique, which can be used to achieve communication performance guarantees with low buffering cost when integrating IPs to network-on-chip architectures.

I. Introduction

The advance of the technology is raising the level of integration of intellectual property (IP) and scalability issue for communication architectures in very large-scale integration systems. Since traditional buses do not scale well in the system-on-chip (SoC) platforms, this trend has driven bus-based architecture toward networks-on-chip (NoCs). Current achievements in integrating more processor cores on a single chip enable to employ these many-core systems as real time multimedia servers. Thus, it is imperative to provide quality of service (QoS) in these systems which have been well available in traditional Internet servers. IPs for a SoC are typically developed concurrently using a standard interface e.g., advanced extensible interface or open core protocol. Despite the standard interfaces, integrating IPs into a SoC infrastructure presents challenges because: 1) traffic flows from IPs are diverse and typically have stringent performance constraints; 2) the impact of interferences among traffic flows is hard to analyze; and 3) of the cost and power constraint, buffers in the SoC infrastructure must not be over-dimensioned while still satisfying performance requirements even under worst-case conditions.

IP integration problem. Master IPs send read and write requests to slave IPs which respond with read data and write acknowledgments. The admission of traffic flows from master IPs into the SoC infrastructure can be controlled by a regulator rather than injecting them as soon as possible. Thus, we can control QoS and achieve cost-effective communication. To lay a solid foundation of the approach, our flow regulation has been based on network calculus. By importing and extending the analytical methods from network calculus, we can obtain worst-case delay and backlog bounds. In we implemented the microarchitecture of the regulator and quantified its hardware speed and cost. The aim of this paper is to optimize the regulator parameters including peak rate and traffic burstiness of flows by formulating optimization problems. Silicon area and power consumption are two critical design challenges for NoC architectures. The network buffers take up a significant part of the NoC area and power consumption consequently, the size of buffers in the system should be minimized. On the contrary, buffers should be large enough to improve communication performance. This means that there is a trade off between buffer size and performance metrics. Hence, we address an optimization problem of minimizing the total number of buffers subject to the performance constraints of the applications running on the SoC. Moreover, since reusing similar or identical switches facilitates the design process of NoC based systems, we formulate another optimization problem to minimize the variances of buffer size in the respective output buffers of switches. As both of the mentioned objective functions are worthwhile for the design process, we formulate them as a multi objective problem under QoS constraints. Finally, we show the benefits of the proposed method and quantify performance improvement and buffer size and variance reduction. Cruz and Chang have pioneered the network calculus, which is a mathematical framework to derive worst case bounds on maximum latency, backlog, and minimum throughput. In a general latency-rate server model was proposed for analyzing traffic scheduling algorithms. Based on this model, they derived deterministic delay and backlog bounds. Le Boudec and Thiran summarized the results of network calculus and their applications in Internet and ATM. Real-time calculus, close to network calculus, was developed for platform-based embedded systems. It generalizes standard event models via upper and lower arrival curves, and processing-element models via upper and lower service curves. Based on these curves, it derives delay and backlog bounds.

II. Literature Review

The authors in [2] proposed a network calculus-based flow regulation and defined a regulation spectrum as a design instrument for SoC architects to control QoS. In this paper, we use the concept of regulation and regulation spectrum in [2] and address the issue of optimal regulation for buffer optimization. We optimize the regulator parameters including peak rate and traffic burstiness of flows

by formulating optimization problems. We propose (σ, ρ)-based flow regulation as a design instrument for System-on-Chip (SoC) architects to control quality-of-service and achieve cost-effective communication, where σ bounds the traffic burstiness and ρ the traffic rate. This regulation changes the burstiness and timing of traffic flows, and can be used to decrease delay and reduce buffer requirements in the SoC infrastructure. In this paper, we define and analyze the regulation spectrum, which bounds the upper and lower limits of regulation. Experiments on a Network-on-Chip (NoC) with guaranteed service demonstrate the benefits of regulation. We conclude that flow regulation may exert significant positive impact on communication performance and buffer requirements**.**

III.Existing System

In traffic shaping was existing as a traffic regulation technique to deal with the QoS IP integration problem. As SoC applications typically do not allow dropping packets, lossless regulation is essential. In regulation spectrum was formally defined to give a valid range for regulation parameters so as to shape (σ , ρ) flows without data loss. It is also shown that this spectrum can be exploited to improve delay and reduce backlog bounds. Because different flows may have conflicting regulation requirements due to sharing network resources, the problem of optimized regulation arises. In the regulation problem was formulated with buffer optimization as objectives, and significant reduction in packet delay and required buffers can be achieved by solving the optimization problem. Both works dealt with static regulation, requiring the characterization of traffic flows (σ , ρ) values offline at design time. Though offline characterization methods such as static traffic analysis and trace-based profiling are possible, they are inflexible and cannot capture traffic dynamism oronly partially. Recently, dynamic traffic characterization and prediction has received increasing attention, thanks to its potential in guiding quality system design.

IV.Proposed System

In this paper, based on the (σ, ρ) regulation model, we elaborate two different traffic regulation schemes for MPSoCs and CMPs, namely, open-loop regulation for MPSoCs and closed-loop regulation for CMPs. The adaptations are needed because of different requirements and contexts of the two different kinds of systems. We have presented two dynamic traffic regulation schemes in a unified framework, which can flexibly adjust regulationstrength on demand. As a result, they make more efficient use of the system interconnect, achieving significant reduction in network packet delay and improving system throughput. While the central idea on traffic admission is the same, the two schemes are applied to different contexts for MPSoC and CMP designs.These regulation techniques are, however, often static, likely causing overregulation and under regulation. We propose dynamic traffic regulation to improve the system performance for NoC-based multi/many-processor systems on- chip (MPSoC) and chip multi/many-core processor (CMP) designs. It can be applied to MPSoCs for intellectual property integration in an open-loop fashion by injecting traffic according to its run-time profiled characteristics. It can also be applied to CMPs in a closed-loop fashion by admitting traffic fully adaptive to the traffic and network states.

Our modification work, to implement the weighted base adaptive circuit switching technique for data transmission process. Then to analysis the shortest path for 3*3 router architecture designs. But some of stuck at faults presented in network on chip architecture, so we include the ECC technique through node to node data transmission process. Error correction codes (ECCs) have been used for decades to protect memories from soft errors. Single error correction (SEC)

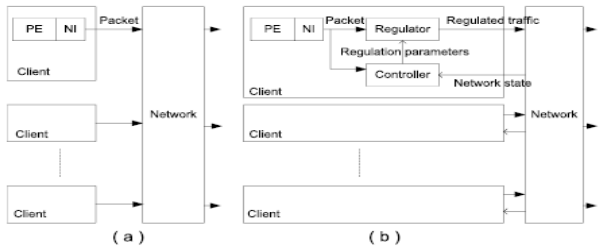
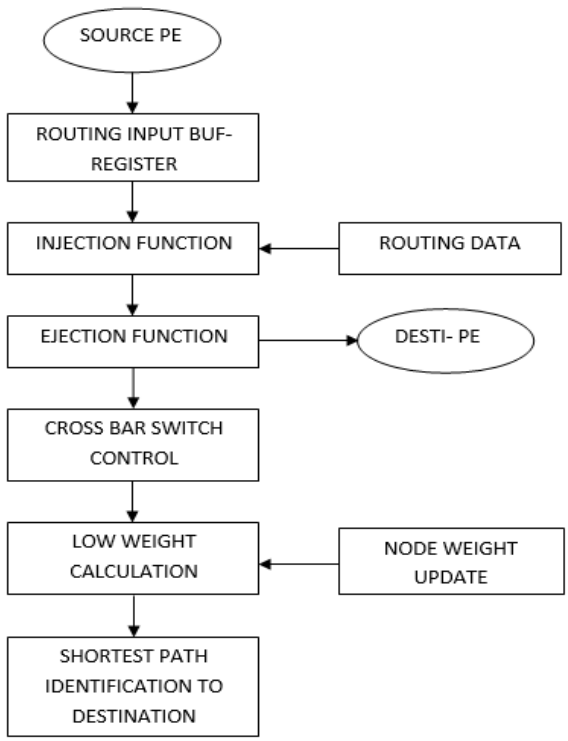


Fig. 1. Traffic injection from client to network (a) without regulation and (b) with regulation.

codes that can correct 1-bit error per word are a common option for memory protection. In some cases, SEC codes are extended to also provide double error detection and are known as SEC-DED codes. As technology scales, soft errors on registers also became a concern and, therefore, SEC codes are used to protect registers. The use of an ECC impacts the circuit design in terms of both delay and area. Traditional SEC or SEC-DED codes developed for memories have focused on minimizing the number of redundant bits added by the code.

WORK FLOW:



this paper we have focused on the output buffers of switches, our method can be easily adapted to input buffers, too.

V.Results

Flow Status	Successful - Wed Nov 01 01:06:15 2006
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	nn
Top-level Entity Name	top_noc_app2
Family	Cyclone III
Device	EP3C40F780C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	3,319 / 39,600 (8 %)
Total combinational functions	2,389 / 39,600 (6 %)
Dedicated logic registers	2,754 / 39,600 (7 %)
Total registers	2754
Total pins	41 / 536 (8 %)
Total virtual pins	0
Total memory bits	256 / 1,161,216 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 252 (0 %)
Total PLLs	0 / 4 (0 %)

Figure2: Area Report

	Fmax	Restricted Fmax	Clock Name	Note
1	250.38 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Figure 5.2: Clock Frequency

PowerPlay Power Analyzer Status	Successful - Wed Nov 01 01:11:52 2006
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	nn
Top-level Entity Name	top_noc_app2
Family	Cyclone III
Device	EP3C40F780C6
Power Models	Final
Total Thermal Power Dissipation	108.37 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	89.05 mW
I/O Thermal Power Dissipation	19.32 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure3: Power analyser report

VI. Conclusion

IP integration requires the provision of performance guarantees for traffic flows and efficient buffer imensioning techniques. The regulation changes the burstiness and timing of traffic flows, and thus can be used to control delay and reduce buffer requirements in the SoC. Since a larger fraction of the NoC cost is due to the network buffers, minimizing buffer requirements is an important problem to achieve an efficient NoC implementation. Also, designing similar switches, as far as possible, facilitates the design process of NoC-based systems. The regulation analysis is performed for best effort packet switching networks. We have also demonstrated that the proposed model exerts significant impact on communication performance and buffer requirements. The algorithm for solving the proposed minimization problems runs very fast. For the case studies, the optimized solution is found within seconds. Although in

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