Design Of FIR Filter Using RoBA(Rounding Based Approximate) Multiplier With Parallel Prefix Adder

M.Sivakami[1] (cvsaii28@gmail.com) ,PG Scholar, Gnanamani College of Technology .
Mr.N.Karthick M.E(kavikarthi.n56@gmail.com), Assistant Professor, Department of ECE, Gnanamani College of Technology.

ABSTRACT
A Novel Rounding Basedapproximate multiplier approach is to round the operands to the nearest exponent of two. This way the computational intensive part of the multiplication is omitted improving speed and energy consumption at the price of a small error. The proposed approach is applicable to both signed and unsigned multiplications. I propose three hardware implementations of the approximate multiplier that includes one for the unsigned and two for the signed operations. The efficiency of the proposed multiplier is evaluated by comparing its performance with those of some approximate and accurate multipliers using different design parameters. The proposed architecture of this paper analysis the logic size, area and power consumption using Synthesis Tools.

I. Introduction

A multiplier is one of the key hardware blocks in most digital signalprocessing (DSP) systems. Typical DSP applications where a multiplier plays animportant role include digital filtering, digital communications and spectralanalysis (Ayman.A et al (2001)). Many current DSP applications are targeted atportable, battery-operated systems, so that power dissipation becomes one of theprimary design constraints. Since multipliers are rather complex circuits and must
typically operate at a high system clock rate, reducing the Delay of a multiplier isan essential part of satisfying the overall design.Multiplications are very expensive and slows the over all operation. Theperformance of many computational problems are often dominated by the speed at which a multiplication operation can be executed. Consider two unsigned binary numbers X and Y that are M and N bits wide, respectively. To introduce the multiplication operation, it is useful to express X and Y in the binary representation

$$X = \Sigma\, Xi\, 2^{i} \qquad i = 0 \text{ to } M \qquad (1.1)$$

$$Y = \Sigma\, Yj\, 2^{j} \qquad j = 0 \text{ to } N \qquad (1.2)$$

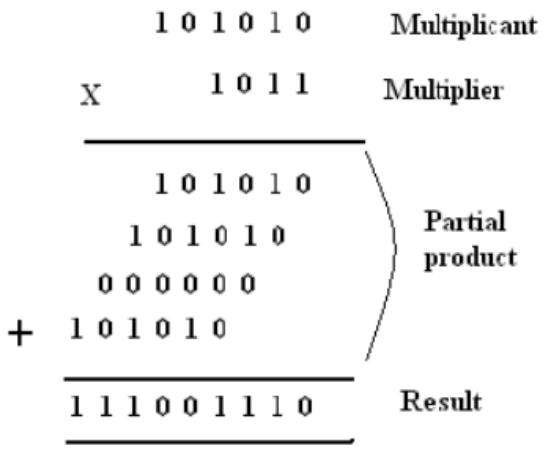
With Xi , Yj Є {0,1}. The multiplication operation is then defined as follows:

$$Z = X \times Y = \Sigma\, Zk\, 2k \quad k = 0 \text{ to } M + N - 1 \qquad (1.3)$$

$$= (\Sigma\, Xi\, 2i \; i = 0 \text{ to } M)\,(\Sigma\, Yj\, 2j \; j = 0 \text{ to } N) \qquad (1.4)$$

$$= \Sigma\,(\Sigma\, Xi\, Yj\, 2i+j) \; i = 0 \text{ to } M-1,\; j = 0 \text{ to } N-1 \qquad (1.5)$$

The simplest way to perform a multiplication is to use a single two
input adder. For inputs that are M and N bits wide, the multiplication tasks M
cycles, using an N-bit adder. This shift –and-add algorithm for multiplication adds together M partial products. Each partial product is generated by multiplying the multiplicand with a bit of the multiplier – which, essentially, is an AND operation – and by shifting the result in the basis of the multiplier bit's position.



II. Literature Review

Inexact (or approximate) computing is an attractiveparadigm for digital processing at nanometric scales.Inexact computing is particularly interesting forcomputer arithmetic designs. This paper deals with theanalysis and design of two new approximate 4-2compressors for utilization in a multiplier. Thesedesigns rely on different features of compression, such that imprecision in computation (as measured by theerror rate and the so-called normalized error distance)can meet with respect to circuit-based figures of meritof a design (number of transistors, delay and powerconsumption). Four different schemes for utilizing theproposed approximate compressors are proposed andanalyzed for a Dadda multiplier. Extensive simulationresults are provided using show that the proposed designs accomplish significantreductions in delay and area compared to an exactdesign.

III.Existing System

The International Technology Roadmap for Semiconductors (ITRS) [1] has anticipated imprecise/approximate designs that became a state-of-the art demand for the emerging class

of killer applications that manifest inherent error-resilience such as multimedia, graphics, and wireless communications.

In the error-resilience systems, adders and multipliers are used as basic building blocks and their approximate designs have attracted significant research interest recently.

Fig. . Wallace Tree for approximate 8 × 8 partial product evaluation

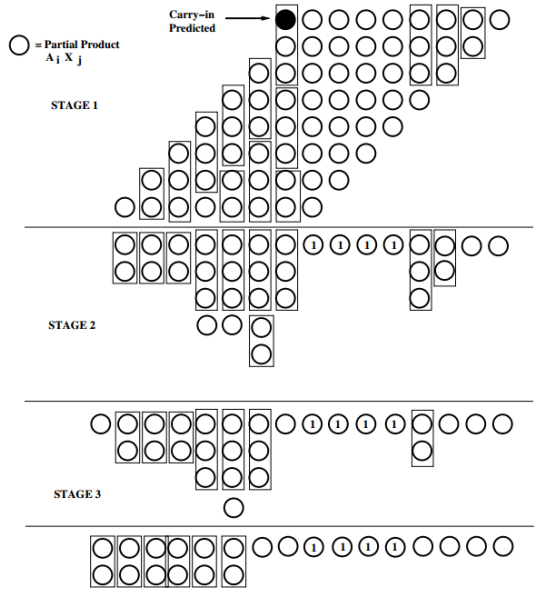


Fig. . Wallace Tree for approximate 8 × 8 partial product evaluation

Conventional wisdom investigated several mechanisms such as truncation over-clocking, and voltage over-scaling(VOS) which could not configure accuracy as well as Latency-Power-Area (LPA) design metrics effectively. Most of the other design techniques rely on functional approximations and a wide. However, very few research papers are reported on approximate multipliers in the literature. Most of the approximate multiplier designs reported shorten the carry-chains in which error is configurable and the algorithms employed in the designs are for smaller numbers and give large magnitude of error as the bit-width of operands increases. present a new Approximate Wallace Tree Multiplier (AWTM) based on a bit-width aware algorithm. I design it specifically to give good results for large operands. Besides accuracy, the AWTM is also optimized for power and area. For single cycle implementation, AWTM gives significant reduction in latency as well. Our contributions are: propose a new power and area-efficient AWTM based on a bit-width aware multiplication algorithm. employ a novel Carry-in Prediction technique which significantly reduces the critical path of our multiplier. further derive an efficient carry-in pre computation logic to accelerate the carry propagation. Complex Design, High hardware requirement also delay is high for large value multiplication

IV.Proposed System

Multiplication Algorithm of RoBA Multiplier

The main idea behind the proposed approximate multiplier is to make use of the ease of operation when the numbers are two to the power n ($2n$). To elaborate on the operation of the approximate multiplier, first, let us denote the rounded numbers of the input of A and B by Ar and Br, respectively. The multiplication of A by B may be rewritten as

$$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br.$$

The key observation is that the multiplications of $Ar \times Br$, $Ar \times B$, and $Br \times A$ may be implemented just by the shift operation. The hardware implementation of $(Ar - A) \times (Br - B)$, however, is rather complex. The weight of this term in the final result, which depends on differences of the exact numbers from their rounded ones, is typically small. Hence, helping simplify the multiplication operation. Hence, to perform the multiplication process, the following expression is used:

$$A \times B \sim = Ar \times B + Br \times A - Ar \times Br .$$

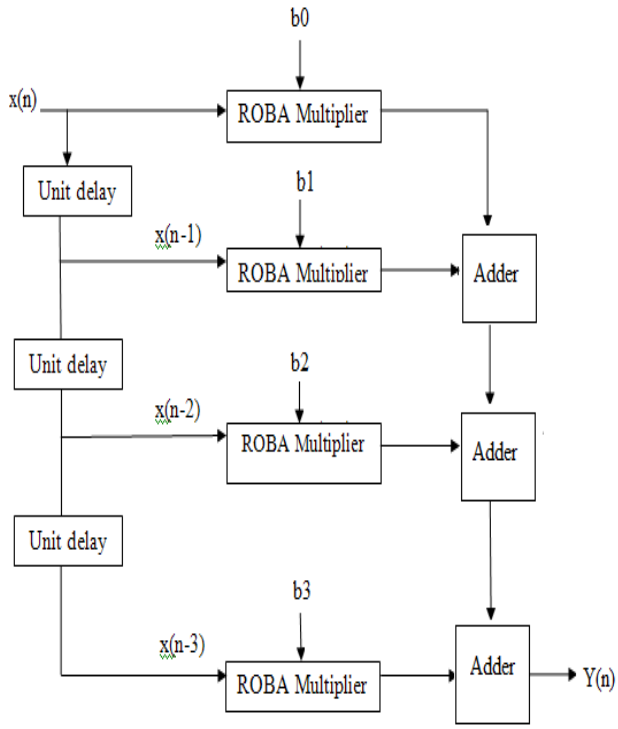


Figure 1 : Block diagram of FIR filter with RoBA multiplier

FIR filter design

In signal processing, there are many instances in which an input signal to a system contains extra unnecessary content or additional noise which can degrade the quality of the desired portion. In such cases, we may remove or filter out the useless samples. Therefore, common filtering objectives are to improve the quality of a signal, to extract information from signals or to separate two or more signals previously combined to make efficient use of an available communication channel. In the FIR system, the impulse response is of finite duration, this means that it has a finite number of nonzero terms. The response of the FIR filter depends only on the present and past input samples.

V.Results

Synthesis results

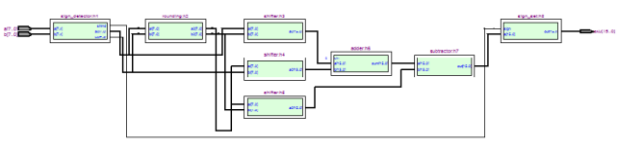


Figure 2 ROBA Hardware Implementation

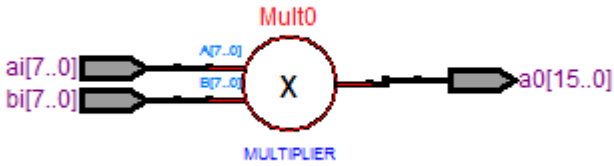


Figure3Shifter

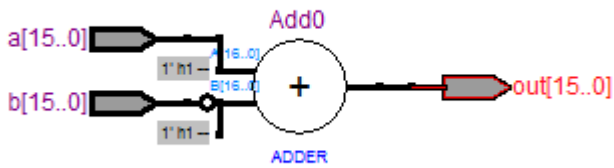


Figure 4 Adder

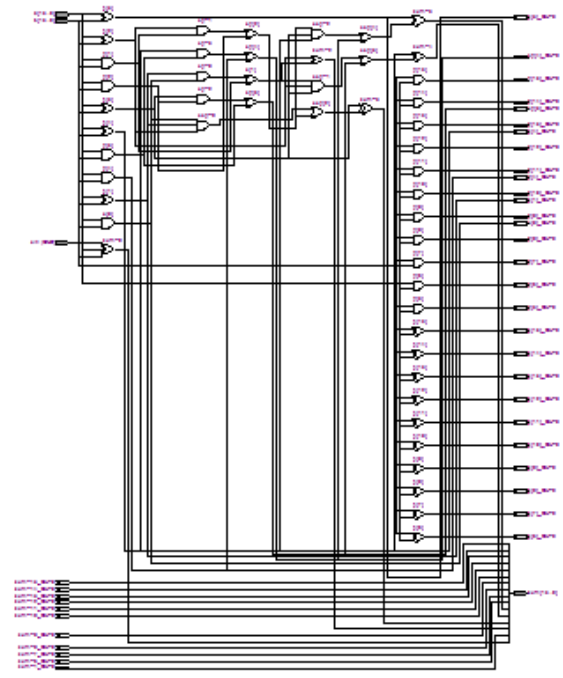


Figure5 Kogge Stone Adder

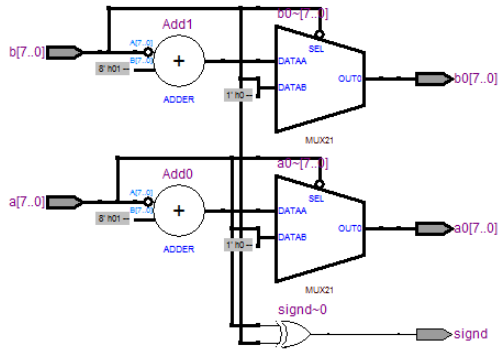


Figure 6Sign Detector

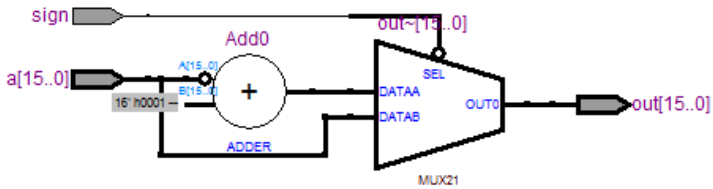


Figure7Sign Set

Timing Analyzer

Actual Time	From	To
23.642ns	B	Bxa
23.639ns	A	Bxa

Powe

r analayzer

Total Thermal Power dissipation	113.67mW
I/O Power dissipation	33.74mW
Core Static thermal power Dissipation	79.94mW

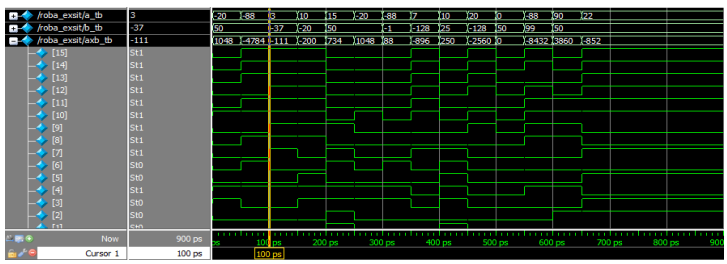


Figure8Waveform For ROBA Multiplier

VI. Conclusion

The proposed multiplier, which had high accuracy, was based on rounding of the inputs in the form of $2n$. In this way, the computational intensive part of the multiplication was omitted improving speed and energy consumption at the price of a small error. The proposed approach was applicable

to both signed and unsigned multiplications. Three hardware implementations of the approximate multiplier including one for the unsigned and two for the signed operations were discussed. The efficiencies of the proposed multipliers were evaluated by comparing them with those of some accurate and approximate multipliers using different design parameters. Also, the efficacy of the proposed approximate multiplication approach was studied in two image processing applications of sharpening and smoothing. The comparison revealed the same image qualities as those of exact multiplication algorithms.

REFERENCES

[1] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.
[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.
[3] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.
[4] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "MACACO: Modeling and analysis of circuits for approximate computing," in Proc. Int. Conf. Comput.-Aided Design, Nov. 2011, pp. 667–673.
[5] F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, "New approximate multiplier for low power digital signal processing," in Proc. 17th Int. Symp. Comput. Archit. Digit. Syst. (CADS), Oct. 2013, pp. 25–30.
[6] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in Proc. 24th Int. Conf. VLSI Design, Jan. 2011, pp. 346–351.
[7] D. R. Kelly, B. J. Phillips, and S. Al-Sarawi, "Approximate signed binary integer multipliers for arithmetic data value speculation," in Proc. Conf. Design Archit. Signal Image Process., 2009, pp. 97–104.
[8] K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC), Dec. 2010, pp. 1–4.
[9] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," IEEE Trans. Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015.
[10] K. Bhardwaj and P. S. Mane, "ACMA: Accuracy-configurable multiplier architecture for error-resilient system-on-chip," in Proc. 8th Int. Workshop Reconfigurable Commun.-Centric Syst.-Chip, 2013, pp. 1–6.