A Fault Tolerance Technique for Combinational and Sequential Circuits using Triple Modular Redundancy Technique

Mr. Sripathi.G, (sripathiyuvi@gmail.com)PG Scholar, AVS Engineering College,Salem, Tamilnadu
Ms. C.Senthilkumar, (ececsk@gmail.com),Assistant Professor, AVS Engineering College,Salem, Tamilnadu.
Mr. G.Kanagaraj, (raj.techstorm@gmail.com), Assistant Professor, AVS Engineering College, Salem, Tamilnadu.

ABSTRACT
Reliability is one of the most critical factors that have to be considered during the designing phase of any IC. In critical applications like Medical equipment & Military applications this reliability factor plays a very critical role in determining the acceptance of product. Insertion of special modules in the main design for reliability enhancement will give considerable amount of area & power penalty. So, a novel approach to this problem is to find ways for reusing the already available components in digital system in efficient way to implement recoverable methodologies. Triple Modular Redundancy (TMR) has traditionally used for protecting digital logic from the SEUs (single event upset) by triplicating the critical components of the system to give fault tolerance to system. TMR technique provides recovery for all internal faults. Hence, proposed design will be more efficient & reliable to use in critical applications, than any other design present till today.

I. Introduction

Reliability with respect to soft errors has become a critical issue in digital circuits. In the past few decades, CMOS technology has reached high scaling advancement. This advancement is consistent with Moore's law, which states that the number of transistors that can be placed in a chip doubles every 18 months. As CMOS technology is reaching the nanometer scale, quantum mechanical effects cause many challenges for additional scaling of CMOS devices. Soft errors are transient errors that can cause digital circuits to operate incorrectly. Soft errors are mainly caused by cosmic-ray neutrons or alpha particles in device packaging. If these particles strike sensitive areas of the circuit, they may result in transientglitches at primary outputs. In previous generations of packaging technology, the effect of soft errors caused by alpha particles can be almost neglected.

Hardware redundancy methods are based on adding redundant hardware to maximize the masking of errors. Triple Modular Redundancy (TMR) is one of the most well-known hardware redundancy techniques. TMR consists of three functionally identical copies of the original circuit that feed a 2-outof-3 majority voter. TMR suffers from high overhead in terms of area and power (more than 200%). In this technique, a module is used to select the correct result, based on the history index of correct computation (HICC). Instead of using merely majority voting to transmit results, the HICC module uses the history indices of redundant units to transmit the correct computation. The most reliable unit is the unit with the highest history index. A generalized modular redundancy scheme is proposed for enhancing the fault tolerance of combinational circuits. In this technique, only the output combinations of the circuit with a high probability of occurrence are protected. This limited protection reduces area overhead compared to TMR. In synthesis-based techniques, a combinational circuit is restructured to maximize the masking properties of a circuit. Logical masking is the main masking property to be maximized. In the logical masking of errors is increased by taking advantage of conditions already present in the circuit, such as observability don't-care terms. Observability don't-care terms are input conditions that will make the output of a circuit not observable. Two techniques are used to improve reliability: don't care-based re-synthesis, and local rewriting. In the first method, high-impact nodes are identified. A node has high impact if many observable faults flow through it. High-impact nodes are used to select areas of the circuit for restructuring, in which a vulnerable node is replicated by adding a single gate. Local rewriting is also used to optimize small sub-circuits to obtain overall area improvements. In two algorithms are proposed to improve input error resilience. They focus on input error due to propagated failures from previous blocks. Both algorithms determine 0–1 assignments for the most critical don't-care terms.

II. Literature survey

To overcome the drawbacks of QL and QT[3], a hybrid design using QT in QL is proposed to enhance the gates that generate the primary outputs in a QL circuit. In a QLQT implementation of the benchmark C17, for example, the two NAND gates at the last logic layer are implemented using QT. This provides a significant advantage over QL. However, a critical error at the third last layer that would be corrected in QL, may not be necessarily corrected in a QLQT circuit; this is caused by the fan-outs of the subcritical errors induced at the second last layer onto the last QT structures. However, these errors may not cause an erroneous output due to: 1) the errors may propagate to two transistors that are not in parallel in QT; and 2) the errors may be corrected by other signals due to their subcritical nature.

Iii. Existing system

Triple modular redundancy has been used in order to design the fault tolerant ALU system. In this process the ALU system carried out is triplicated, each having the same input, thus making it triple mode redundant. The output of all the three ALUs is passed onto the Voting Circuit which contrasts the outputs and then passes the majority output. It means that if any two ALUs are giving the similar output, then that output will be passed by the voting circuit and that

turns out to be the final output of the entire circuit. In case of all the ALUs giving the similar outputs, then that output becomes the last output but in case of all the three ALUs giving dissimilar outputs then the voting circuit faces a dilemma and it fails. At this time the final output is undefined.

IV. Proposed system

An alternative way to have a fault less system is Fault Tolerant System, Triple Modular Redundancy (TMR) is used for making a fault tolerant system for Multiplexer, DFF, Binary to gray code converter. FPGA platform used in Altera Cyclone kit and Altera Quartus software is for functional and timing simulation. This model not only detects the faulty processor but also repair the faulty bits in the faulty processor .Fault detection are done over the air means at the same time. By using this TMR model, the faulty processor is detected as well as the administrator will be able to know that fault lie in which bit of which processor.

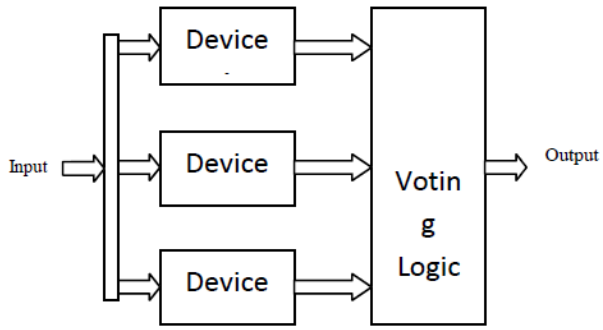

Figure 1 Block Diagram Of Tmr

inside and generate a different output. This inconsistency will be caught and corrected by voting logic .Thus; the voted output is always a correct value under the assumption of single error. Thus, the voted output is always a correct value under the assumption of single error. When the TMR concept is applied to a processor (system), all output signal of the CPU are voted; therefore no error should exist at output of voters. Any error that occurs represent that one of the CPUs has an error inside .If that error is not corrected by some way; it may result in more errors and finally become unrecoverable.

In the design of fault-tolerant systems, the designer must consider the possible occurrence of several different kinds of faults such as transient faults, intermittent faults, permanent, logical faults, and indeterminate faults. Transient faults, often caused by external disturbances, exist for a finite length of time and are nonrecurring. Intermittent faults occur periodically and typically result from unstable device operation. Permanent faults are perpetual and can be caused by physical damage or design errors.

V.Results

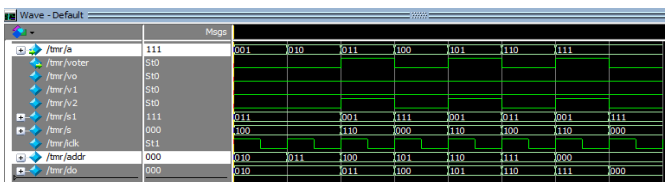

Figure 2 TMR Combinational Logic

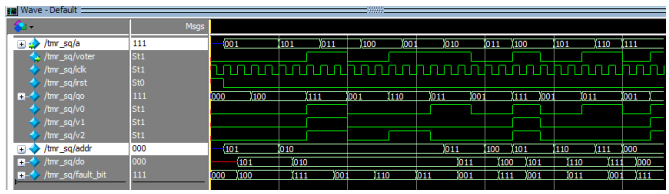

Figure 3 TMR Squential Logic

Flow Status	Successful - Fri Nov 10 19:36:59 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	lut
Top-level Entity Name	lut
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	42 / 33,216 (< 1 %)
Total combinational functions	26 / 33,216 (< 1 %)
Dedicated logic registers	30 / 33,216 (< 1 %)
Total registers	30
Total pins	13 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 4Area Report

PowerPlay Power Analyzer Status	Successful - Fri Nov 10 19:33:46 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	lut
Top-level Entity Name	lut
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	111.40 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	79.93 mW
I/O Thermal Power Dissipation	31.47 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 5 Power Report

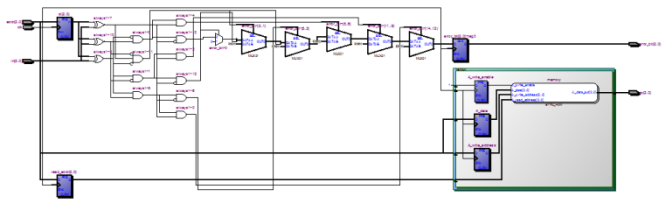

Figure 6 RTL View Fault Tolerant

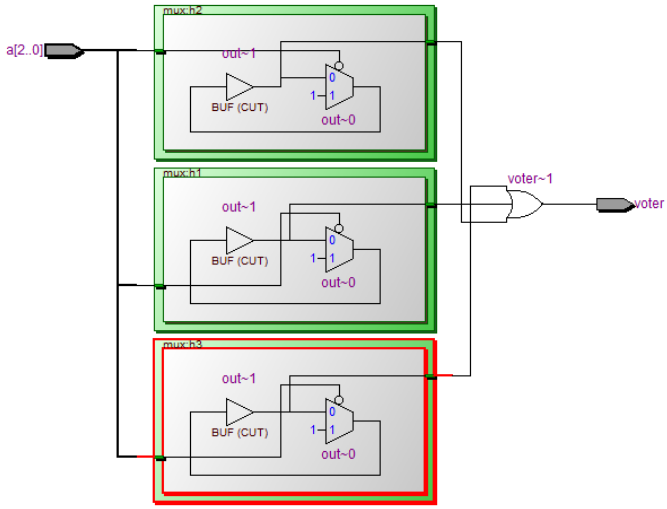

Figure 7 TMR For Combinational Logic

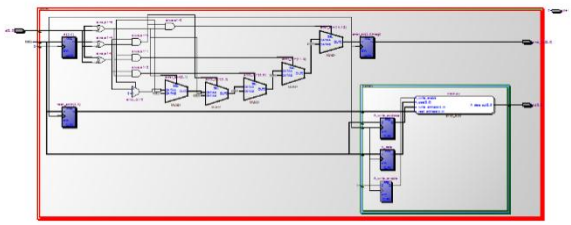

Figure 8 TMR For Squential Logic

VI. Conclusion

TMR-based ALU fault tolerance technique for combinational circuits has been discussed in literature papers. This proposed technique can be applied DFF,Multiplexer,code converter to achieve a given circuit reliability or enhance the reliability of a circuit under a given area constraint. This system evaluates the processor and checks for the faulty bits in the processor. By evaluating the faults in the processor prevents the whole system from collapsing. With the help of TMR administrator will come to know which of the processor is diverting from regular program and they will able to take the appropriate action based on the results. This system detects the faults in the systems.

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