# Single-Input Dual-Output Three-Level DC–DC Converter for EV

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Abstract— This paper presents the development of a non-isolated single-input dual-output three-level dc-dc converter (SIDO-TLC) appropriate for medium- and high-voltage applications. 3 level Buck-Boost converter is used in order to achieve the controllable output voltages. The main merits of this project include reducing voltage stress across semiconductor devices, improving efficiency, and reducing passive components size. This converter shows very good stability, even under simultaneous step changes of the loads and input voltage. Simulation analysis of converter output voltages for various duty cycles is presented for three cases of duty cycle control range.

Keywords- Multiple converter, single input dual-output dc-dc converter (SIDOC), single-input dual-output three-level dc-dc converter (SIDO-TLC), buck-boost converter

### I. INTRODUCTION

Multi-Output DC-DC converters have attracted increasing interest due to the high demand for energy in many fields and for different applications, such as supplying different loads at the same time and the integration of renewable energy sources (photovoltaic panels, wind turbine, etc.) in micro-grids. At higher voltages, switches voltage stress is a major challenge for multiport dc-dc converters. The reason for that are the issues such as the cost and the inaccessibility of high-voltage switches, which could also have a negative effect on overall efficiency. The project is about designing a high-efficiency multiport dc-dc converter with reduced voltage stress across semiconductor devices and shrunken passive components size. K. Filsoof and P. W. Lehn [2] proposed a bidirectional multiple-input multipleoutput modular multilevel DC-DC converter and its control design. In this converter, the voltage stress on switches is shared among the levels. In addition to its complex control system, the converter is not capable of generating buck and boost output voltages at the same time. As a result, it requires two separate circuits with different topologies to generate each voltage separately. O. Ray, A. P. Josyula, S. Mishra, and A. Joshi [3] proposed integrated dual-output converter. Proposed converter which one of its outputs is boost and the other one is buck at the same time. The converter is appropriate for low-voltage applications. Meanwhile, because of high voltage stress on the diode and the series added switches, and also due to the lack of proper high input current distribution among the switches, the converter's both conduction and switching losses are high, which can lead to a fairly low system efficiency. SEPIC based dual output DC-DC converter for solar applications is proposed in [4]. The converter which is a combination of the SEPIC and five-level boost converters is composed of one switch and ten diodes. The voltage stress on the switch is reduced to one-fifth of the high voltage side. Yet, high number of diodes may effect the reliability of the system. Moreover, reducing the passive components size, which is one of the advantages of the multilevel structures, has not been achieved through the proposed converter.

This paper presents the modeling and performance of single-input dual-output DC-DC converter. Simulation results are presented to demonstrate the buck and boost utput voltage ranges under three cases of duty cycle control range.

# II. SINGLE- INPUT DUAL- OUTPUT THREE- LEVEL DC- DC CONVERTER

Fig. 1 shows the circuit diagram of the Single- Input Dual-Output Three- Level DC-DC Converter. In Fig. 1,  $V_{in}$  is the input voltage,  $V_{o1}$  is the step-up output voltage,  $V_{o2}$  is the step- down output voltage. The series capacitors  $C_{11}$  and  $C_{12}$  are the filter capacitors of the step-up output, while  $C_2$  is that the filter capacitor of the step-down output. The converter consists of 4 power switches:  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , with antiparallel diodes, and two power diodes:  $D_{11}$  and  $D_{12}$ .  $V_{ab}$  is that the unfiltered step-down output voltage,  $V_{L1}$  and  $V_{L2}$  are the instantaneous voltages of inductors,  $i_{C11}$  and  $i_{C12}$  are the currents of the series capacitors,  $i_{C2}$  is the current through the step-down capacitor  $C_2$ , and  $V_{C11}$ ,  $V_{C22}$  are the voltages of the series capacitors and  $V_{C2}$  is the voltage of the step-down capacitor.

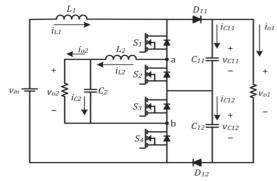


Fig. 1. Circuit Diagram of SIDO-TLC

### A. Switching States of Single- Input Dual-Output Three-Level DC-DC Converter

Table I shows the switching states, the unfiltered step-down output voltage  $V_{ab}$ , the instantaneous voltages of inductors  $V_{LI}$  and  $V_{L2}$ , the currents of series capacitors  $i_{CII}$  and  $i_{CI2}$ , and also the voltage change (direction) of capacitors.

### B. Operating Range of Single-Input Dual-Output Three-Level DC-DC Converter

Regarding the duty cycles of the switches, there are three possible operating cases named A, B, and C for the SIDO-TLC. In the ideal situation, the control signals of  $S_1$  and  $S_4$  have the same duty cycles ( $d_{SI} = d_{S4} = d_1$ ) and are 180° phase shifted. In the same way, the control signals of  $S_2$  and  $S_3$  have the same duty cycles ( $d_{S2} = d_{S3} = d_2$ ) and are 180° phase shifted. Depending on  $d_1$  and  $d_2$  values, the operating cases can be expressed as follows:

Case A:  $(1/2 < d_1 \text{ and } d_2 < 1) \text{ and } (d_1 > d_2)$ Case B:  $(1/2 < d_1 \text{ and } d_2 < 1) \text{ and } (d_1 < d_2)$ Case C:  $(d_2 + 1/2 < d_1 < 1) \text{ and } (0 < d_2 < 1/2).$ 

TABLE I. OPERATING RANGE OF THE SIDO-TLC

Switching States	$S_I$	$S_2$	$S_3$	$S_4$	$V_{ab}$	$V_{L1}$	$V_{L2}$	$i_{c11}$	$i_{c12}$	C <sub>11</sub>	$C_{12}$
1	0	0	0	0							
2	0	0	1	0	0	$V_{in}$ - $V_{ol}$	$-V_{o2}$	$i_{Ll}$ - $V_{\alpha l}/R_{\alpha l}$	$i_{LI}$ - $v_{ol}/R_{ol}$	<b>↑</b>	<b>↑</b>
3	0	1	0	0	Ü	vin vol	V 02	ili vojitoj	LI VOI/ NOI		ı
4	0	1	1	0							
5	0	0	1	1	0	$V_{in}$ - $V_{ol}/2$	$-V_{o2}$	$i_{LI}$ - $v_{\alpha I}/R_{\alpha I}$	$-V_{ol}/R_{ol}$	<b>↑</b>	1
6	0	1	1	1	•	rin rorz	* 02	tLI volvitoi	, 0h 1.01	ı	<b>+</b>
7	1	1	0	0	0	$V_{in}$ - $V_{ol}/2$	$-V_{o2}$	$-V_{ol}/R_{ol}$	$i_{LI}$ - $v_{oI}/R_{oI}$	1	<b>↑</b>
8	1	1	1	0		· in · or 2	* 02	* 01 <sup>,</sup> 2201	-L1 · 01/01	<b>+</b>	ı
9	0	0	0	1	$V_{ol}/2$	$V_{in}$ - $V_{o1}$	$V_{01}/2-V_{02}$	$i_{Ll}$ - $v_{ol}/R_{ol}$	$i_{L1}$ - $i_{L2}$ - $V_{o1}/R_{o1}$	<b>1</b> 1	<b>↑</b>
10	0	1	0	1	· 07 =	7 th 7 01	7 01 = 7 02	-L1 - 0101	*E1 *E2 * 01 = -01	' '	
11	1	0	0	0	$V_{ol}/2$	$V_{in}$ - $V_{ol}$	$V_{ol}/2-V_{o2}$	$i_{L1}$ - $i_{L2}$ - $V_{ol}/R_{ol}$	$i_{Ll}$ - $v_{ol}/R_{ol}$	<b>↑</b>	↑ ↑
12	1	0	1	0	· 07 =	· in · 01	· 0F = · 02	*E1 *E2 * 0F **-01	-L1 · 0F01	'	1 1
13	1	0	1	1	$V_{ol}/2$	$V_{in}$ - $V_{ol}/2$	$V_{o1}/2-V_{o2}$	$i_{L1}$ - $i_{L2}$ - $V_{o1}/R_{o1}$	$-V_{ol}/R_{ol}$	<b>1</b>	$\downarrow$
14	1	1	0	1	$V_{ol}/2$	$V_{in}$ - $V_{ol}/2$	$V_{oI}/2-V_{o2}$	$-V_{ol}/R_{ol}$	$i_{L1}$ - $i_{L2}$ - $V_{o1}/R_{o1}$	$\downarrow$	$\uparrow$
15	1	0	0	1	$V_{oI}$	$V_{in}$ - $V_{oI}$	$V_{oI}$ - $V_{o2}$	$i_{L1}$ - $i_{L2}$ - $V_{o1}/R_{o1}$	$i_{L1}$ - $i_{L2}$ - $V_{o1}/R_{o1}$	1	1
16	1	1	1	1	0	$V_{in}$	$-V_{o2}$	$-V_{ol}/R_{ol}$	$-V_{ol}/R_{ol}$	$\downarrow$	$\downarrow$

TABLE II. OPERATING RANGE OF THE SIDO-TLC

CASE	Duty-cycle limits	Voltage limits		
A	$\frac{1}{2} < d_1 \& d_2 < 1$ $d_1 > d_2$	$v_{in/2} < v_{o2} < v_{o1/2}$		
В	$d_1 > d_2$ $d_1 < d_1 & d_2 < 1$ $d_1 < d_2$	$0 < v_{o2} < v_{in/2}$ $v_{o1} > 2(v_{in} - v_{o2})$		
С	$d_2 + \frac{1}{2} < d_1 < 1$ $0 < d_2 < \frac{1}{2}$	$v_{o1/2} < v_{o2} < v_{01}$ $v_{in} < v_{o1} < 2v_{in}$		

### C. Waveforms (Different Cases) of Single- Input Dual – Output Three- Level DC- DC Converter

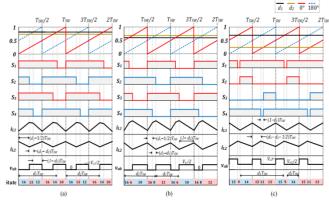


Fig. 2. Typical waveforms of the proposed converter, including the control signals of the switches, inductors currents, unfiltered step-down output voltage vab, and the switching states for all operating cases: (a) case A, (b) case B, and (c) case C

### III. MATHEMATICAL MODELING OF SIDO-TLC

According to switching states of SIDO-TDC and the switching sequences in waveforms, the output voltage's conversion ratio can be obtained.

### A. Case A:

For inductor  $L_1$ ,

$$\frac{V_{in}(d_2-1/2)}{\text{State } 16} + \frac{(V_{in}-V_{o1}/2)(d_1-d_2)}{\text{State } 13} + \frac{(V_{in}-V_{o1})(1-d_1)}{\text{State } 12} = 0$$

 $V_{in}(d_2) - V_{in}/2 + V_{in}(d_1) - V_{in}(d_2) - V_{oI}(d_1)/2 + V_{oI}(d_2)/2 + V_{in} - V_{in}(d_1) - V_{oI} + V_{oI}(d_1) = 0$ 

$$V_{in} = V_{ol}(2-d_1-d_2)$$

$$V_{ol}/V_{in} = (1/2 - d_1 - d_2)$$
 (1)

Therefore, Step-up voltage gain =  $V_{ol}/V_{in}=1/(2-d_1-d_2)$ .

For inductor  $L_2$ ,

$$\frac{(-V_{o2})(d_2-1/2)+(V_{o1}/2-V_{o2})(d_1-d_2)+(V_{o1}/2-V_{o2})(1-d_1)}{\text{state } 16 \qquad \text{state } 13 \qquad \text{state } 12}$$

$$\begin{array}{l} -V_{o2}(d_2) + V_{o2}/2 + V_{o1}(d_1)/2 - V_{o1}(d_2)/2 - V_{o2}(d_1) + V_{o2}(d_2) - \\ V_{o1}(d_1)/2 + (V_{o1}/2) - V_{o2} + V_{o2}(d_1) = 0 \end{array}$$

$$V_{o1}(1-d_2) = V_{o2}$$
  
 $V_{o2}/V_{o1} = 1-d_2$  (2)

By doing product of (1) and (2),

$$(V_{ol}/V_{in})*(V_{o2}/V_{ol})=V_{o2}/V_{in}$$

Voltage gain, 
$$V_{o2}/V_{in} = (1-d_2)/(2-d_1-d_2)$$
 (3)

#### B. Case B:

The voltage gains in cases B and C can also be achieved in the same way as the above procedure.

For inductor  $L_1$ ,

Step-up voltage gain = 
$$V_{ol}/V_{in}=1/(2-d_1-d_2)$$
 (4)

For inductor  $L_2$ ,

Step-down voltage gain = 
$$V_{o2}/V_{in} = (1-d_2)/(2-d_1-d_2)$$
 (5)

### C. Case C:

For inductor  $L_1$ ,

Step-up voltage gain = 
$$V_{ol}/V_{in}$$
=1/(1-d2) (6)

For inductor  $L_2$ ,

Step-down voltage gain = 
$$V_{o2}/V_{in} = (d_1 - d_2)/(1 - d_2)$$
 (7)

# IV. EFFECT OF MODULATION INDEX ON THE CONVERTER OUTPUT VOLTAGE

Simulation of SIDO-TLC is performed in Matlab-Simulink environment. This DC-DC converter is tested for the above three cases: CaseA, CaseB & CaseC for various duty cycle. Each case is explained below. Fig. 3, Fig. 4, Fig. 5, and Fig. 6 are obtained from the Tables III, IV, and V in which the

### Analysis of SIDO-TLC under Case A

The range of duty cycle for the converter under Case A is:  $(1/2 < d_1 \text{ and } d_2 < 1, d_1 > d_2)$ . Simulation is performed by keeping  $d_1$ =0.8 and  $d_2$  is varied from 0.4 to 0.8. The dual output voltages  $V_{01}$  and  $V_{02}$  of the converter is tabulated in Table III.  $V_{01}$  and  $V_{02}$  are calculated using (1)-(3). It is observed that  $V_{01}$  gives step-up voltage and gives step-down voltage. Variation of  $V_{01}$  with  $d_2$  for given values of  $d_1$  is shown in Fig. 3. It is observed that  $V_{01}$  increases with increase in duty cycles. When the graph is plotted for  $V_{o2}$  by keeping  $d_1$  constant and varying  $d_2$ , the negative slope curve is obtained (i.e., the  $V_{o2}$  values kept on decreasing).

TABLE III. SIMULATION AND THEORETICAL VALUES OF  $V_{\rm o1}~\&~V_{\rm o2}$  by VARYING D2 AND FIXED D1 UNDER CASE A WITH D1=0.9

Duty Cycle	Simul val		Theoritical values		
$d_2$	V <sub>o1</sub> (V)	(V)	(V)	(V)	
0.8	349.8	38.2	199.99	39.99	
0.7	274.0	42.8	149.99	44.99	
0.6	222.1	48.6	120.0	47.99	
0.5	185.3	52.5	99.99	49.99	
0.4	184.6	54.9	85.7	51.4	



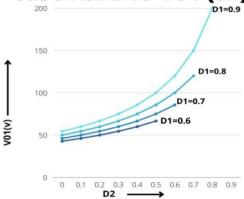


Fig. 3. Graph for d2 Vs vo1(th)

### case A:(D2 vs Vo2 )(th)

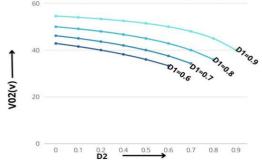


Fig. 4. Graph for d<sub>2</sub> Vs v<sub>o2</sub>(th)

### B. Analysis of SIDO-TLC under Case B

The range of duty cycle for the converter under Case B is:  $(1/2 < d_1 \text{ and } d_2 < 1, d_1 < d_2)$ . Simulation is performed by keeping d1=0.7 and d2 is varied from 0.75 to 0.95. The dual Fig. 6. Graph for d1 Vs vo2(th) output voltages  $V_{01}$  and  $V_{02}$  of the converter is tabulated in

theoretical and simulation values of step-up output voltages Table IV.  $V_{01}$  and  $V_{02}$  are calculated using (4) and (5). Variation and step-down output voltages are mentioned for 3 different of  $V_{0I}$  with  $d_2$  for given values of  $d_1$  is shown in Fig. 5. It is observed that  $V_{01}$  increases with increase in duty cycles.

TABLE IV. SIMULATION AND THEORETICAL VALUES OF  $V_{\rm o1}~\&~V_{\rm o2}$  by Varying  $D_2$  and Fixed  $D_1$  under Case A with  $D_1=0.7$ 

Duty cycle		lation lues	Theoritical values		
$d_2$	(V)	$V_{o2}$ (V)	(V)	(V)	
0.9	220.8	4.765	120.0	12.0	
0.8	190.2	8.706	100.0	20.0	
0.7	167.7	15.28	85.71	25.71	

### Case B : D1 vs vo1(th)

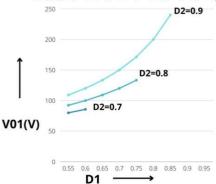


Fig. 5. Graph for  $d_1\ Vs\ V_{\rm ol}(th)$ 

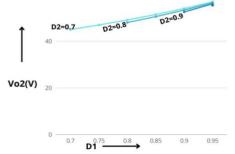
### Analysis of SIDO-TLC under Case C

The range of duty cycle for the converter under Case B is:  $(d_2 + 1/2 < d_1 < 1, 0 < d_2 < 1/2)$ . Simulation is performed by keeping  $d_2$ =0.2 and  $d_1$  is varied from 0.8 to 0.95. The dual output voltages  $V_{01}$  and  $V_{02}$  of the converter is tabulated in Table V.  $V_{01}$  and  $V_{02}$  are calculated using (6) and (7). Variation of  $V_{02}$  with  $d_1$  for given values of  $d_2$  is shown in Fig. 6. When the graph is plotted for the  $V_{o2}$  by varying  $d_1$  and keeping  $d_2$ constant, the positive transient curve is obtained (i.e., the  $V_{o2}$ values kept on increasing).

TABLE V. SIMULATION AND THEORETICAL VALUES OF  $V_{o1}$  &  $V_{o2}$  BY VARYING D<sub>2</sub> AND FIXED D<sub>1</sub>

Duty cycle		lation lues	Theoritical values		
$d_1$	$V_{oI}$ (V)	V <sub>o2</sub> (V)	(V)	(V)	
0.8	138	55.59	60	48	
0.85	138	52.74	63.15	50.52	
0.9	138.6	53.39	66.66	53.33	
0.95	138.7	42.63	70.58	56.47	

## case C:D1 vs Vo2(th)



### V. CONCLUSION

This paper presents a high-efficiency non-isolated SIDO-TLC, whose outputs are boost and buck simultaneous. The converter is appropriate for medium- and high-voltage applications. The controllable output voltages are obtained with the help of three-level buck-boost converter. The advantages of this converter include its high efficiency, reduced passive components size and the reduced voltage stress across the semiconductor devices. The proposed converter finds its applications in electric vehicle, solar PV systems and the systems which require the multi output. This converter shows very good stability, even under simultaneous step changes of the loads and input voltage.

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