Multilevel Inverter with Self-Balanced Capacitor for Electric Vehicle Application

Dandu Moulika
Electrical & Electronics Engineering Department
Kakatiya Institute of Technology & Science
Warangal, Telangana, India.
moulidandu98@gmail.com

C. Venkatesh
Electrical & Electronics Engineering Department
Kakatiya Institute of Technology & Science
Warangal, Telangana, India.
cv.eee@kitsw.ac.in

***Abstract*— A new three-phase multilevel inverter with boosting capacity for low-voltage applications such as electric vehicles and renewable energy sources is described in this article. Two low-voltage transistors, two high-voltage transistors, two diodes, and two capacitors are used in each phase of this inverter, which is powered by a single dc voltage source. All other components are rated to the dc input voltage, with the exception of the two high-voltage transistors, which can tolerate double the dc input voltage. The two types of high and low-voltage transistors work in low and high switching frequencies, respectively, using phase-disposition pulse width modulation. This is highly useful for decreasing switching losses and semiconductor switches are being chosen. The two capacitors are linked to the dc source in parallel and series alternatively, yielding a high ac output voltage with various levels, self-balanced capacitor voltages, and low voltage ripples. The topology, working principle, voltage ripples are examined. The SCMLI topology is demonstrated using MATLAB/simulink software.**

Keywords*— Pulse width modulation (PWM), multilevel inverter (MLI), switched-capacitor

I. INTRODUCTION

With the quick advancement of electric vehicles (EVs) and sustainable power sources (RES, for example, sunlight based chargers and energy units), supporting sort inverters are turning out to be progressively significant in low-voltage applications where the low voltage of a dc source should be helped and afterward modified to a high ac voltage to drive an engine of Electric vehicle (or) interface with the framework. Course supporting sort dc-dc converters with an ordinary two-level inverter is the popularized answer for this kind of inverter. All semiconductors in the two-level inverter should get through high voltage and work at a high exchanging recurrence in this framework, bringing about expanded exchanging misfortune and a significant EMI issue happens. Another kind of MLI in view of exchanged capacitor (SC) innovation has been acquainted all together with address this issue[1].

SC based MLIs (SCMLIs) are primarily developed for low-voltage applications, as opposed to NPC, FC, CHB, and MMC, which have been commercialized in medium- and high-voltage applications. They have the advantages of voltage-boosting capabilities and self-balanced capacitor voltages. Furthermore, without the usage of additional balancing circuits or control algorithms, the voltages of all capacitors in this SCMLI are automatically balanced.

The low voltage of a single dc source is converted to three-phase high ac voltages with four levels per phase using a SCMLI with motor applications was developed in this paper. The suggested three-phase SCMLI is not appropriate for high-voltage applications since each phase includes two transistors that tolerate twice the input voltage. Voltage-boosting capability, simple circuit configuration, and self-balanced capacitor voltages are all advantages.

These characteristics suggest mostly employed for low-voltage applications such as electric vehicles, solar panels, and fuel cells, rather than a competitor of traditional MLIs[2][3]. Two types of high-voltage and low-voltage transistors used in the SCMLI operate in low and high switching frequencies, respectively, with phase-disposition pulse-width modulation (PD-PWM)[4]. Induction motors are appealing choices for traction applications because of their sturdy architecture, wide field weakening range, low cost, and high durability. IM is more reliable than other types of electric motors, which is especially important for EVs, PHEVs, and HEVs that require a high-power motor. Squirrel enclosure the most common type of induction motor utilized for traction purposes is the induction machine[8]. The motor is controlled by an inverter in order to deliver the required torque for a certain driving circumstance at a specific speed.

So, that switching loss is reduced. Moreover, capacitor's voltage ripples and the harmonics of output voltages are reduced as well. This paper presents about the THD of the inverter output current and voltage between the series R-load, RL-load, RLC and Motor application to SCMLI is determined by using the MATLAB/Simulink software.

II. TOPOLOGY OF SCMLI

A. Circuit Description

Fig. 1 illustrates the single-phase SCMLI. Its three phases use the same circuit and are powered by a dc voltage source, V_{dc}. Two dc-link capacitors C_1 and C_2 provide the neutral point, each having a 0.5 V_{dc} voltage stress. When compared to a two-level half-bridge inverter, between the dc supply and the inverting half-bridge, each phase of the inverter has an additional SC unit. One half-bridge, two diodes, and two capacitors make up the SC component. As a result, each phase of the SCMLI employs two half-bridges, with each half-bridge consisting of two complementary functioning transistors.

The capacitor C_x is charged by the dc source through the diode D_x when the transistor T_x is turned on while T'_x is off, where x = 1, 2, and 3. The capacitor voltage V_{cx} is now equal to V_{dc}. When T'_x is turned on while T_x is turned off, C'_x is charged to V_{dc} through D'_x. The dc input voltage V_{dc} is rated for all components in this SC unit.

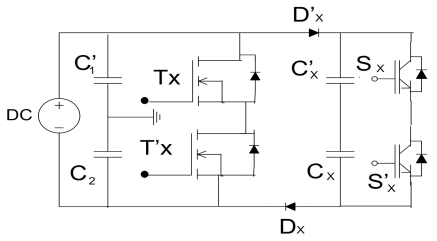


Fig.1. circuit diagram of SCMLI

Furthermore, the inverting half-bridge is connected in parallel with C_x and C'_x series connection. As a result, the voltage stress on S_x and S'_x is $2V_{dc}$. Each of them can alternatively be built using two series-connected transistors, ensuring that the SCMLI's entire component set is rated toV_{dc}.

B. Principle of operation

To make the analysis easier, all of the components of SCMLI are treated as ideal, and the Capacitors C_1, C_2, $C_x$and C'_x are more that their voltages are constant at $0.5V_{dc}$ and V_{dc}, respectively. There are four switching states in total, as shown in Table I, because each half-bridge is controlled by a pair of complimentary signals and each phase has two half-bridges. It's worth noting that 1 and 0 correspond to the ON and OFF states of the associated transistor, respectively.

TABLE I SWITCHING STATES OF SCMLI

Switching states	Switches				Capacitors		Output
	T_X	T'_X	S_X	S'_X	C_X	C'_X	u_s
1	1	0	1	0	C	D	$+1.5V_{dc}$
2	0	1	1	0	-	C	$+0.5V_{dc}$
3	1	0	0	1	C	-	$-0.5V_{dc}$
4	0	1	0	1	D	C	$-1.5V_{dc}$

The states of capacitors are denoted by the letters "C," "D," and "--" which stands for charging, discharging, and idle conditions, respectively. As a result, the suggested inverter may produce four different output levels: $\pm 0.5V_{dc}$, $\pm 1.5V_{dc}$, In comparison to the typical two-level inverter, which can only generate levels of $0.5V_{dc}$ on each phase, the suggested inverter not only boosts but also generates more ac voltage levels.

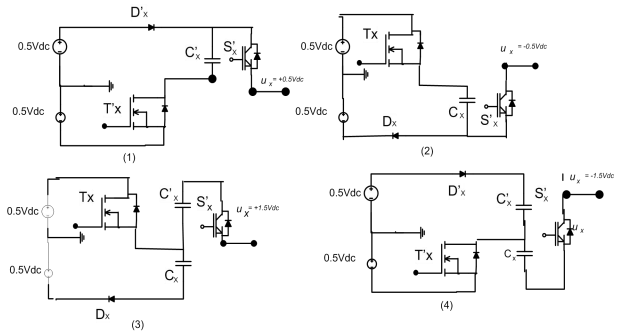


Fig. 2. Principle of operation of SCMLI

- $u_x = +0.5V_{dc}$*:* When the switches S_x and T'_x are turned on while T_x and S'_x are off, the capacitor C_1 provides the output level $+0.5V_{dc}$ directly through the diode D'_x and the switch S_x, as shown in Fig. 2. (1). For inductive loads, the reverse series connection of and C_2 can yield the same output level. C'_x gets charged by the dc source while C_x is idle in this state.
- $u_x = -0.5V_{dc}$*:* When the switches T_x and S'_x are switched on while S_x and T'_x are off, C_2 provides a direct output level of $-0.5V_{dc}$ via the diode D_x and the switch S'_x, as shown in Fig. 2. (2). For inductive loads, the reverse series connection of C_1 and C_x can yield the same output level. C_x gets charged by the dc source while C'_x is idle in this state.
- $u_x = +1.5V_{dc}$*:* The output level $+1.5V_{dc}$ is provided by the series connection of C_1 and C'_x when the switches S_x and T_x are turned ON while S'_x and T'_x are OFF, as illustrated in Fig. 2. (3). C_x is charged by the dc source in this state, and C'_x discharges to loads.
- $u_x = 1.5V_{dc}$*:* The output level of $1.5V_{dc}$ is produced by the series connection of C_2 and C_x when the switched S'_x and T'_x are turned on while S_x and T_x are off, as illustrated in Fig. 2(4). The dc source charges C'_x, and C_x discharges to loads in this state.

C. Switched Capacitor Voltages Self-Balancing of SCMLI

The transistors T_x and T'_x operates in a complimentary manner and the capacitors C'_x and C_x are alternately charged and discharged by the dc source through the diodes D_x and D'_x. As a result, their voltages are automatically balanced to the V_{dc} of dc input voltage. Therefore the voltage balancing itself is done due to the switched capacitors. These capacitors also reduce the THD by balancing itself the output voltage distortion.

D. Multilevel output voltage generation mode

However, the charged capacitors should be discharged in series in order to produce output voltage and a staircase waveform with the desired frequency and amplitude. The suggested switched-capacitors multilevel inverter's simplicity and adaptability allow for a relatively simple switching technique to provide staircase voltage that is four level output voltage in this article.

III. MODULATION STRATEGY

To regulate the output voltage of the SCMLI, the PD-PWM method is used in which three triangular carrier signals are compared to a sinusoidal 50Hz reference signal to create needed pulses for switches in this section to demonstrate how the SCMLI works with the motor applications like electric vehicle.

The modulation logic and representative waveforms of the three-phase SCMLI with the PD-PWM method are shown in Figs. 3 and 4. The gating signals $V_{G\_S_{1,2,3}}$ and $V_{G\_T_{1,2,3}}$ are generated by comparing the three carrier signals u_1, u_2 , and u_3 to the reference signals u_{ref_a}, u_{ref_b}, and u_{ref_c}.

Yet again the gating signals $V_{G\_S_x}$ are shaped by contrasting the reference signal u_{ref_x} , and the bipolar transporter signal u_1, where x = 1, 2, and 3. When $u_{ref\_x} > u_2$ or $u_1 > u_{ref\_x} > u_3$, the semiconductor T_x is turned ON, as per Table I. As an outcome, $V_{G\_T_x}$ its gating signal is the after effect of contrasting the reference signal and the three transporters as displayed in Fig 4.

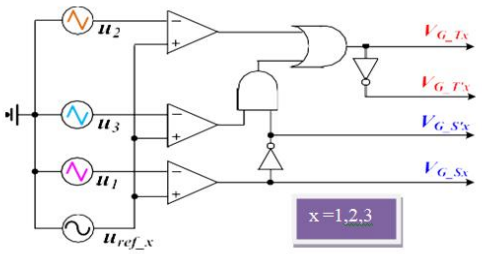


Fig. 3. Modulation logic of PD-PWM

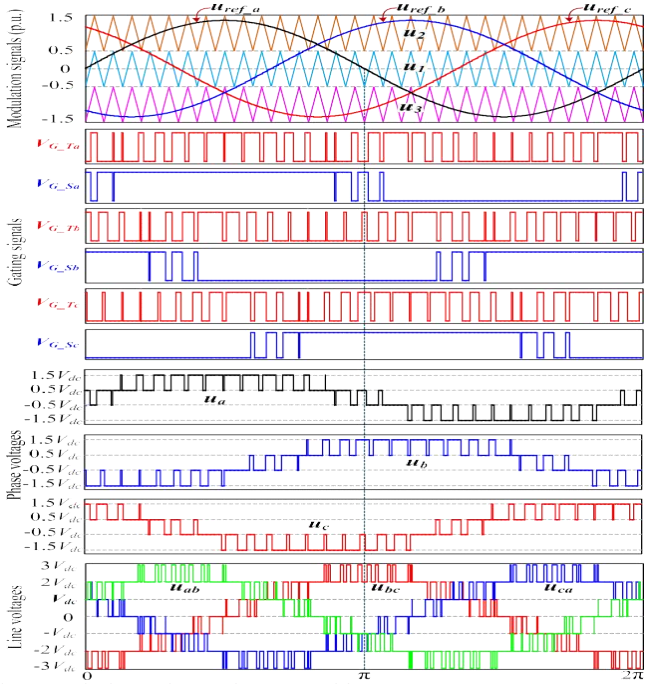


Fig. 4. Typical waveforms of SCMLI with PD-PWM.

The waveforms in Fig. 4 demonstrate that the high-voltage transistors $S_{1,2,3}$ and $S'_{1,2,3}$ have a lower switching frequency than the low-voltage transistors $T_{1,2,3}$ and $T'_{1,2,3}$. This is highly useful for transistor selection and switching loss minimization. Low-voltage transistors, for example, can be MOSFETs with low ON-resistance and quick turn-on/off speed, whereas high-voltage transistors can be IGBTs.

As a consequence, as shown in Fig. 4, there are seven possible levels for the SCMLI's line voltages u_{ab}, u_{bc}, and u_{ca}. The line voltages have an amplitude three times that of the dc input voltage, or $3V_{dc}$. The line voltages are therefore closer to sinusoidal waveforms than with a traditional two-level inverter, and the three-phase inverter may be powered with a low dc voltage source.

IV. Calculation of Capacitance

SCMLI, the SCs C_x and C'_x are employed as dc voltage sources to provide different levels of output voltages. When they are discharged to loads, their will be a small amount of voltages drop. The capacitors in the PD-PWM switch between power conversion modes (charging and discharging) at the carriers' frequency. Voltage ripples of C_x and C'_x in three different scenarios are shown as the influence of the overall parasitic resistance r_{Cr}, which includes the ESR of capacitors, on-resistance of switches, and the internal impedance of the dc source.

The signal u_{ref_x} achieves its maximum amplitude A_{ref}, which is $r_{Cr}C_x$ (1.5 - A_{ref})/(4 f_C), where f_C is the carrier frequency. The integral of the load current i_x and the duty ratio d for each charging interval, as well as the capacitance, can be seen as steady in each period of carrier frequency under the assumption that the carriers frequency is much higher than the reference signals' frequency, and the capacitors' voltage ripples are determined by the integral of the load current i_x and the duty ratio d for each charging interval i.e.,

$$\Delta V_{cx} = \frac{Q_x}{C_x} = \frac{i_x(t) \times d(t)}{C_x f_C}$$

$$= \frac{I_o(\sin(\omega t - \varphi)}{C_x f_C} [A_{ref} \sin(\omega t) - 0.5] \qquad (1)$$

where I_o = the amplitude of the current,
ω = angular frequency of the output current, and
φ = phase difference between the output voltage and output current.

The maximal voltage ripple ΔV_{Cmax} is obtained in the interval when u_{ref_x} reaches its amplitude A_{ref} for loads with a power factor of 1. During this discharging phase, the output current also approaches I_o.

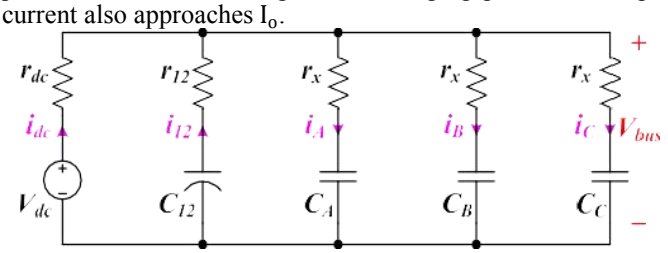


Fig. 5. Capacitor charging network for three-phase operation

In each stage, one SC is connected in equal all the time with the dc source to charge all of a sudden, as displayed in Fig 2. where in C_A, C_B and C_C represent three SCs are associated in corresponding with the dc source and dc-connect capacitors for three-stage activity. The ESR of the DC-connect capacitors is $C_{12} = \frac{C_1}{2} = \frac{C_2}{2}$, r_{12}, C_{12}, where r_{dc} is the dc source's inner impedance, r_x is the amount of ESR for every one of C_x and C'_x, and ON-opposition for every one of T_x and T'_x and r_x is the complete of ESR for every one of T_x and T'_x. The virtual transport voltage V_{bus} might be determined by setting $r_{dc} = k \times r_{12}$ and utilizing the Kirchhoff's voltage rule to Fig. 5. The voltage ripple ratio $\frac{\Delta V_{Cmax}}{V_{dc}}$ is generally set to 5% or 10%.

V. Simulation Analysis of SCMLI

The boosting element of the inverter permits it to change over low dc input voltage to high ac yield voltage. Classic MLIs, like NPC and FC, do not have the capacity to boost, yet they have been marketed in ac motor drivers with a medium voltage and high power. As a result, it's impossible to make a fair comparison between the suggested inverter and the most common four level MLIs. Performance of 3-phase SCMLI is tested with R-, RL- and motor load.

A. Three-phase SCMLI with R-LOAD

The capacitor's charging currents flowing through the transistors transistor T_x and T'_x rise in tandem with the load currents as more power is required to replace greater voltage ripples of capacitors.

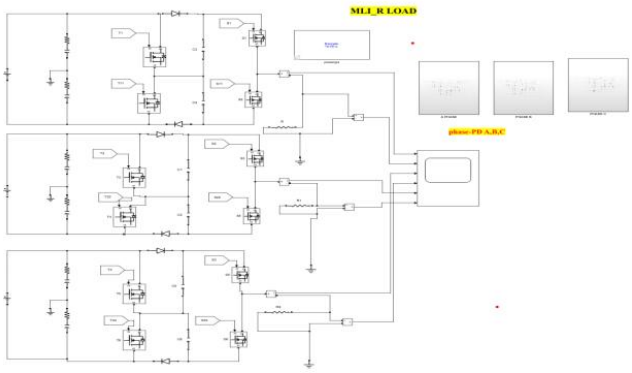


Fig 6. Simulation model of R-load with three-phase SCMLI

The three-phase SCMLI simulation circuit connected to R=100Ω and the modulation index adjusted to 0.933 is shown in Fig. 6. The output phase voltages are u_{a0}', u_{b0}', u_{c0}' respectively. The simulation results of the three-phase SCMLI are shown in Fig. 7. It shows the output phase voltages u_{a0}' i.e., phase-A.

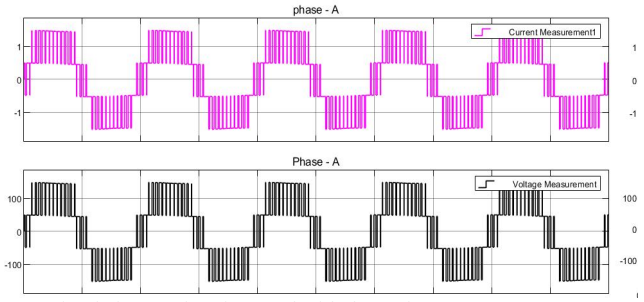


Fig. 7. Simulation results of R-Load with three-phase SCMLI

An LC filter (4.5 mH+4.7μF) is added to suppress the higher harmonics of the output voltage. In order to test the dynamic response of the inverter, the load R is varied in between 100 and 200 Ω. THDs of voltage and current are found reduced. Fig. 10 shows the output voltage and current waveforms of SCMLI with LC filter connected R-load. Table II shows the RMS and THD values of output voltage and currents for different modulation index. It is observed that the current THD is reduced and within the limits of IEEE Std. 519. Fig. 8 depicts the FFT analysis of current waveform.

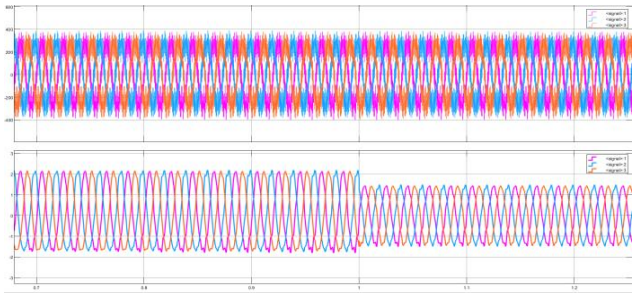


Fig. 10. Simulation results of R-Load with LC filter of three-phase SCMLI

TABLE II THD VALUES OF INVERTER OUTPUT VOLTAGE AND CURRENT WITH R-LOAD WITH LC FILTER

S. No	Modulation index	V_{rms} (V)	I_{rms} (A)	V_{THD} (V)	I_{THD} (A)
1	0.95	270.65	1.38	33.89	1.25
2	0.9	270.22	1.35	33.80	1.30
3	0.85	245.23	1.356	34.09	1.35
4	0.8	225.80	1.25	34.20	1.42
5	0.75	210.50	1.20	34.21	1.42
6	0.7	205.30	1.14	34.25	1.78
7	0.65	195.23	1.02	37.50	2.21
8	0.6	190.1	0.90	37.80	2.30

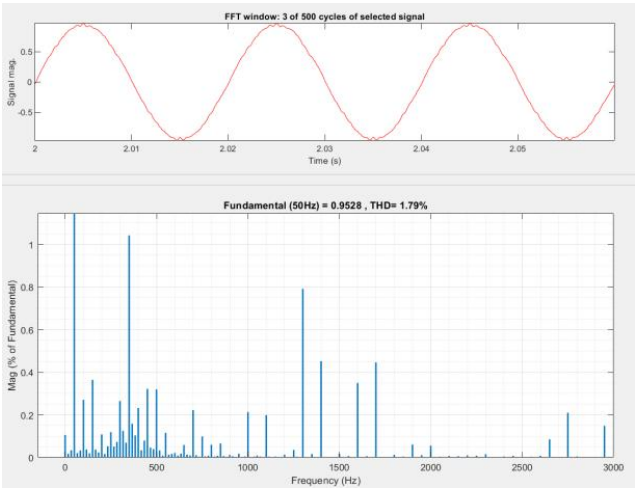


Fig. 8. FFT analysis of output and load voltages of the three-phase four-level inverter With PD-PWM

B. Simulation model three-phase SCMLI with RL-load

Switched capacitor of three-phase with RL-load is analysed. The rms value is roughly 210V, and the carrier frequency of 5 kHz and its integer multiples are mostly the emphasis of the harmonics. The load phase voltages are u_{A0}, u_{B0}, u_{C0} and line voltages are u_{AB}, u_{BC}, u_{CA}. Their relative rms values are around 191V and 331V. Total load voltages, on the other hand, are sinusoidal, with only a few lower harmonics.

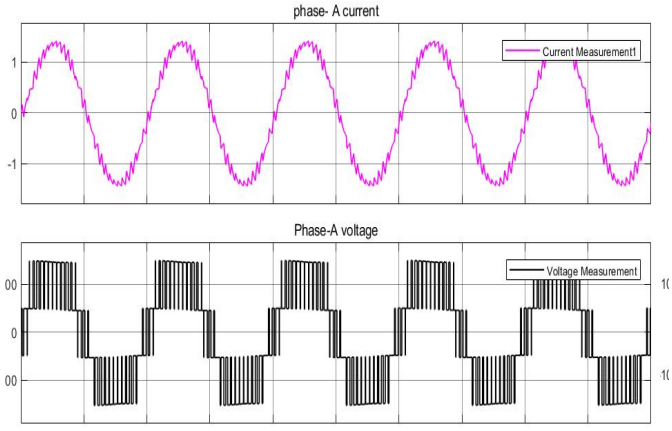
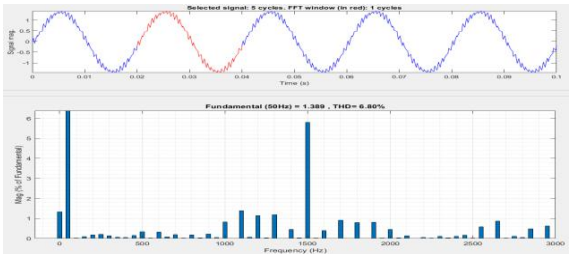
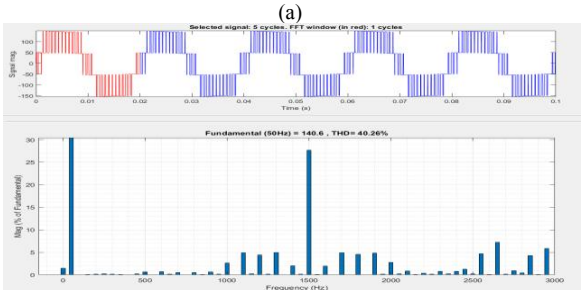


Fig. 9. Simulation results of RL-load with three-phase SCMLI



(a)



(b)

Fig. 10. (a) & (b). FFT analysis of output current and voltage of three-phase four-level SCMLI inverter with R-load

TABLE- III RMS AND THD VALUES OF OUTPUT VOLTAGE AND CURRENT FOR THREE-PHASE SCMLI INVERTER WITH R-LOAD

S. No	Modulation index	V_{rms} (V)	I_{rms} (A)	V_{THD} (V)	I_{THD} (A)
1	0.95	109.08	1.046	40.36	6.80
2	0.9	107.01	0.99	40.36	6.80
3	0.85	102.05	0.93	40.36	6.80
4	0.8	98.17	0.88	40.36	6.80
5	0.75	92.87	0.82	40.36	6.80
6	0.7	88.32	0.77	40.36	6.80
7	0.65	83.13	0.71	40.36	6.80
8	0.6	77.97	0.66	40.36	6.80

Fig. 9 represents that the load currents are practically sinusoidal. Because capacitors absorb the inductive load's reactive power, their voltages can occasionally exceed 200 V, but the ripples are very small. FFT analysis of SCMLI load output voltage and current for RL load is shown in Fig.10. The THD of voltage and current is 40.28% and 6.80% respectively. Modulation index is varied in control circuit to test the performance of the inverter. Table III shows the RMS and THD values of output voltage and current for various modulation indices. It is found that the rms values change with modulation index and the THD values remain same in all the cases. That means it is a good performance of SCMLI. The capacitors are self-balancing and giving the good response.

C. 3-Phase step-up SCMLI with motor application

Advancements in electric machines and power electronics are significant enablers for electric vehicles. Induction motors, (PMSM), PM brushless DC machines (PMSM), and switching reluctance motors (SRMs) have all been used for various vehicle. Brushed DC motors are no longer considered a good choice for traction applications like streetcars due to their massive structure, low efficiency, need for commutator and brush maintenance, high electromagnetic interference (EMI), decreased dependability, and finite speed range. When electric motors are combined with inverters and controllers, they offer a wide speed range for constant torque and a longer speed range for continuous power output, making power-train design much easier.

For electric vehicles, a three-phase step up multilevel inverter with a switching capacitor inverter is used. In this paper the SCMLI performance is tested with induction motor connected as shown on Fig. 11.

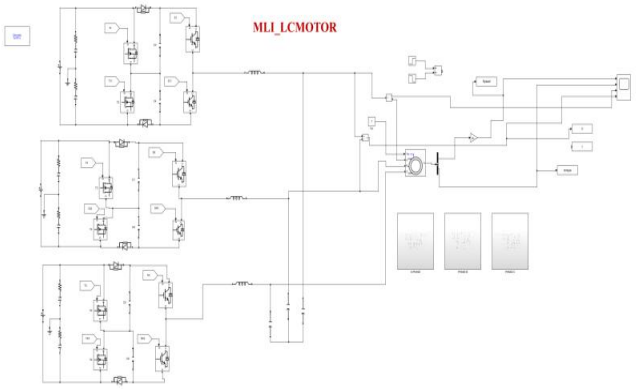


Fig. 11. Three-phase step-up multilevel inverter MLI with motor application

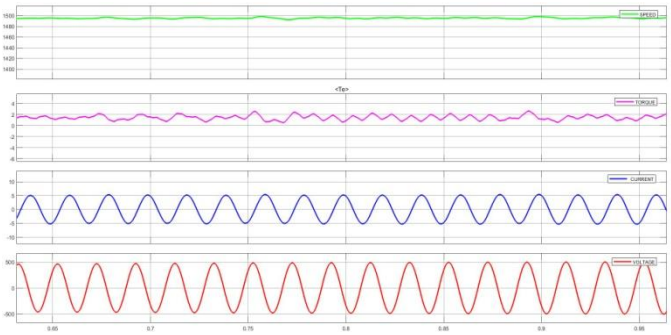


Fig. 12. Simulation result of SCMLI with motor application.

The output voltage and current of SCMLI is pure sinusodial which is having 420volts and 5Amps because of low switching losses there is no variation in the waveforms. The speed is regulated upto 1500rpm which is very good response. Steady state speed is reached in 5 to 6 sec. Hence it also have the fast response in speed regulation.

VI. CONCLUSION

The switching capacitor-based three-phase four-level inverter with self-balancing was examined. The capacitors in the inverter alternate between charging and discharging modes, producing self-balanced voltages with low voltage ripples. They are linked in parallel and series alternatively with a dc voltage source to provide a high ac output voltage with four levels. Simulation result shows that SCMLI gives good performance by adding LC-filter for R-load. With RL-load the SCMLI has given current THDs within the limits. Result with induction motor connected to SCMLI shows that the speed is regulated upto 1500rpm which is very good response. Steady state speed is reached in 5 to 6 sec. Hence it also has the fast response in speed regulation. As a result, low-voltage applications such as EV motor drivers are better suited to it. We can also see in the findings that we can regulate the speed

of an electric car by altering the speed of the motor or adjusting the speed of the motor.

REFERENCES

[1] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878–887, Feb. 2012.

[2] H. Akagi, "Multilevel converters: Fundamental circuits and systems," in Proc. IEEE, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.

[3] K. Wang, Z. Zheng, and Y. Li, "Topology and control of a four-level ANPC inverter," IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2342–2352, Mar. 2020.

[4] L. He and C. Cheng, "A bridge modular switched-capacitor-based multilevel inverter with optimized SPWM control method and enhanced power-decoupling ability," IEEE Trans. Ind. Electron., vol. 65, no. 8, pp. 6140–6149, Aug. 2018.

[5] Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series-parallel conversion with less number of components," IEEE Trans. Ind. Electron., vol. 63, no. 6, pp. 3582–3594, Jun. 2016

[6] M. Habib Ullah, T.S. Gunawan, M. R. Sharif "Design of Environmental Friendly Hybrid Electric Vehicle" International Conference on Computer and Communication Engineering (TCCCE 2012) pp. 544-548.

[7] Shaikh Elan, Apte Aishwarya, "Simulation & Development of Inverter Fed Three Phase Induction Motor Using VIf Control Strategy" International Journal of Emerging Technology and Advanced Engineering pp151-156.

[8] M. K. Kazimierczuk, "Switching losses with linear MOSFET output capacitance," in Pulse-Width Modulated DC–DC Power Converters, 1st ed. West Sussex, U.K.: Wiley, 2008, pp. 37–38, ch. 2, sec. 2.2.9.

[9] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage source inverters," in Proc. 23rd Annu. IEEE Power Electron. Specialists Conf., Jun./Jul. 1992, pp. 397–403.

[10] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel Converters for large Electric Drives," IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 36- 44,Jan./Feb. 1999.

[11] Y. H. Chang, "Design and Analysis of Multistage Multiphase Switched Capacitor Boost DC–AC Inverter" IEEE Trans. Circuits Syst. I, Vol. 58, No. 1, Jan 2011.